Design of a Systolic Pattern Matcher for Nanomagnet Logic

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***Abstract*—Nanomagnet Logic (NML) is widely considered to be one of the promising for "beyond-CMOS" nanoscale architectures. So far only relatively simple circuits (nanomagnetic logic gates and adders) have been studied experimentally and in simulations. Here we investigate the possibility of building larger-scale computing devices from out-of-plane NML. We designed a systolic pattern matcher circuit that is in principle scalable to arbitrary number of nanomagnets and can match arbitrarily long patterns in an incoming data stream. The design of this systolic architecture for NML makes an important step toward large-scale devices.**

Keywords-Nanomagnet Logic; systolic architecture; Co/Pt nanomagnets; micromagnetic simulation;

I. INTRODUCTION

Recently, Cobalt/Platinum (Co/Pt) ultra-thin multilayer-based field-coupled nanomagnets have been proposed as an alternative candidate for Nanomagnet Logic [1] [2] In these devices, due to the material anisotropy, the easy-axis of the nanomagnets lies out-of-plane. Compared with in-plane NML (mainly Permalloy-based NML) [3] [4], Co/Pt nanomagnets offer the benefit that the magnetic properties can be engineered by focused ion beam (FIB) irradiation, which allows us to have another tool in engineering NML devices [5].

With a proper FIB irradiation, artificial nucleation sites can be created at certain parts of the nanomagnets, which can significantly influence the switching mode and also dramatically decrease the switching fields of the magnets. We presented our micromagnetic simulation model of partially irradiation Co/Pt nanomagnets in [6] and [7]. It was verified that with partial FIB irradiation, the most frequently observed "errors" (metastable states) [8] in NML can be effectively eliminated thanks to the asymmetric coupling behavior, and in the end error-free nanomagnetic computing can be achieved [6].

In experiments, the fundamental elements of NML, such as the inverter chains, majority gates and fan-out structures were successfully implemented in [9] [10] [11], verifying the switching of each nanomagnet can be well-controlled by FIB-defined nucleation sites. Experimental work is ongoing toward larger circuits built from several gates.

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In the earlier study, we demonstrated our design of an XOR gate [7]. However, the scalability of NML for larger-size circuits is yet an open question. Circuits with irregular layout are challenging to realize in NML: there is no demonstrated solution for wire-crossing and long-distance nanomagnet-wires have long latency. Nanomagnets naturally lend themselves for the implementation of pipelined architectures. We choose a systolic architecture to demonstrate large scale NML circuitry, which relies heavily on pipelining and does not require irregular gate-to-gate connections. The basic concepts of systolic architecture and particularly the functionality of a systolic pattern matcher (SPM) are outlined in Section II. Section III describes our layout design of an n-bit ($n = 2, 3, 4\ldots$) systolic pattern matcher and section IV is the verification with simulations. In Section V, we sum up the results and draw the conclusions.

II. SYSTOLIC PATTERN MATCHING

The name, systolic array refers to a matrix-like arrangement arrangement of processing elements (PE) [12]. The structure of a systolic array is demonstrated in Fig. 1, where identical PEs compute data and communicate with their neighbors. The task of one PE can be summarized as: receiving data, computing data and transmitting data.

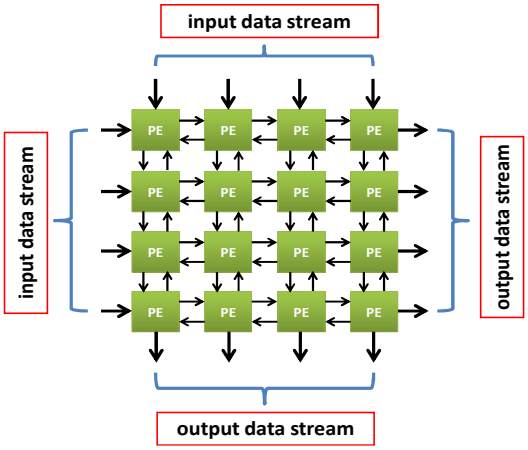

Figure 1. Systolic architecure built from PEs.

As a specific systolic design, systolic pattern matchers are used to find the occurrences of a binary pattern W in an binary input stream X. Fig. 2 illustrates the structure of an n-bit pattern matcher built up from n PEs (n stands for the number of PEs in this SPM and an n-bit SPM is able to match n-bit patterns).

The fundamental PE in a SPM circuit is relatively simple. Each PE consists of one XNOR gate and one AND gate, as shown in the inset of Fig. 2. The elements of the W pattern are stored in such a way that the first bit W_1 is saved in PE_1 (the leftmost), the second bit W_2 in PE_2, and the i-th bit W_i in PE_i. (Notably, we can take advantage of NML's non-volatility to store this bit directly at the gate—with no static power loss. The W bits could possibly be made to be programmable via spin transfer torque (STT).) The input data stream steps in the SPM from left and propagates to right. As soon as the first bit of the input stream arrives at PE_1, the comparison starts. Y_i indicates the global matching history for the first i-bit long segment of X. This global history (Y_1, Y_2 ... Y_n) is then shifted from right to left, and the final output Y_n is read out from PE_n, telling if the n-bit long segment from the input stream matches with the n-bit pattern. The process in each PE can be decomposed into three steps: 1) the i-th PE takes the i-th bit from the input segment X_{in} and sends it to its XNOR gate. 2) the XNOR gate compares this bit with the corresponding W_i pattern bit. The result of the comparison is sent to the AND gate of this PE. 3) the AND gate takes both responses from its XNOR gate and the (i-1)th AND gate (which is Y_{i-1} from the right PE), generates a new response Y_i, and sends it to the next PE ((i+1)th PE on the left side). These three steps repeat n times from PE to PE to achieve output Y_n for this segment. If at any point the output of an XNOR gate is a '0', the accumulated global history is set to '0', which suggests that there is no match in input stream bits X_m … X_{m+n-1}.

If and only if the segment of the X input data is completely matched with the W pattern, the output will be logic '1', otherwise the output will be logic '0'. Subsequent values of the Y_n output indicate match / mismatch for the next n-bit long segments of X_{in}.

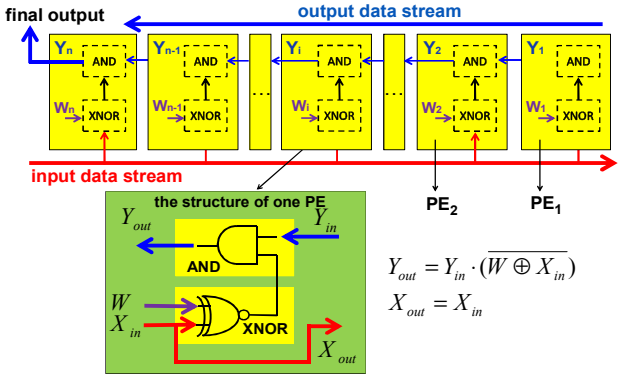

Figure 2. Information flow in an n-bit systolic pattern matcher. The inset shows the two simple components in an processing element: one AND gate and one XNOR gate.

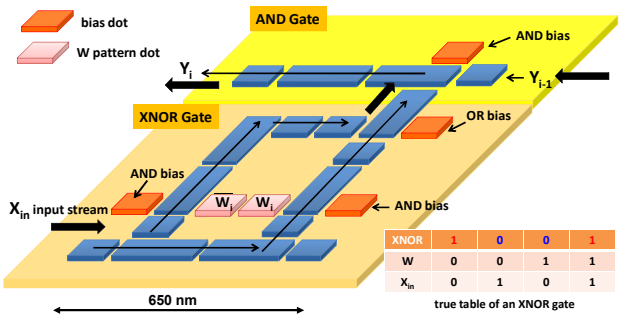

Figure 3. The layout of our designed PE.

III. Design of one Systolic PE

In NML, AND and OR computations can be carried out with majority gates [13], and NOT function can be implemented with a nanomagnet (dot) chain with an even number of dots. In circuit design, information propagation in gates and chains can be ensured by a proper irradiation at the sides of each dot together with an easy-axis external oscillating clock field [6] [7]. The information steps forward two dots after each clocking cycle. Ideally, the layout of a pattern matching PE should (1) facilitate the dense tiling of arbitrary number of PEs on the chip area and (2) all PE outputs should be computed after exactly the same clocking cycles, so that data streams are under control and not mixed up during processing.

Based on the discussion above, our specific design is presented in Fig. 3, where the arrows indicate how the information propagates (the partially irradiated parts of the dots are not shown). Input data come into the structure from the bottom left and final output leaves out from the top left. The pattern to be recognized is stored in dots marked with W_i and the neighboring dot is set to the opposite logic state (two pink ones in Fig. 3). Both of these two dots are with hard magnetization and their state remains fixed during the whole computing. The bottom left dot is the input dot, which receives incoming data and the top right dot is the one, which receives response from the former PE. In our layout, the AND gate (the top part in Fig. 3) is implemented with a majority gate with a bias input, and the XNOR gate (the bottom part in Fig. 3) is realized with three majority gates: two of them function as AND gates and the third one works as an OR gate. We optimized the number of dots in the XNOR gate to improve the operating speed. Compared to the XOR gate (which contains similar components) in [6], this design saves more than 50% area. This design is the most compact so far, which also satisfies the prerequisite 2.

There are two signal paths from the input dot to the output dot of the XNOR gate. But one of the paths is "shut down" when signal passes through the other one, depending on the logic state of pattern bit W_i in this PE_i. Illustrated in Fig. 4, if pattern bit W_i is at logic 0 state, taking into account that this majority gate is an AND gate, the logic state of the other input dot is irrelevant for the output of the AND gate: the right path is blocked and information only flows

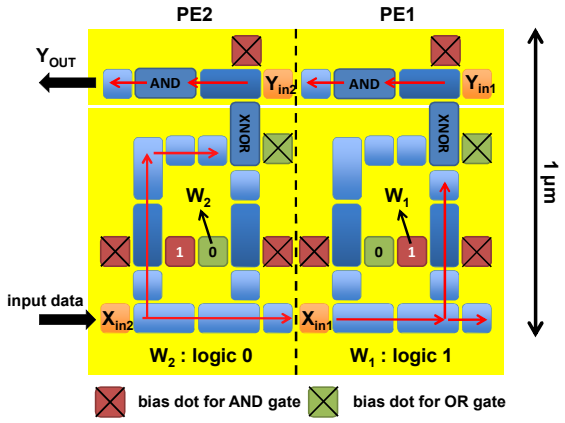

Figure 4. Two neighboring PEs: The pattern bits saved in these two PEs are '1' and '0' respectively, and two information paths are illustrated.

along the left path. Similarly, information only flows in the right path when the logic state of pattern bit is logic 1. With this design, neighboring PEs can be connected directly so that PE-to-PE interconnection does not require additional dots. An *n*-bit SPM can be achieved by putting *n* PEs in a row next to each other.

IV. Timing Constrains in an n-Bit Systolic Pattern Matcher

The time interval between two adjacent input bits in principle should be chosen as short as possible, while keeping the data flow in synchronization. However, given this bi-directional dataflow in the systolic pattern matcher, there are also some architectural-level timing constraints that must be fulfilled. For instance, bits of the input stream must be "spaced" two PEs apart to ensure that global history bits and streaming input data meet at the proper time. In this case, the time interval between two adjacent input bits is 4 oscillating cycles, as shown in Fig. 5.

An obvious detriment to this is that the throughput of the system will be degraded as output bits will also be spaced two PEs apart. However, there is no reason that two different input streams cannot be interleaved within the systolic array.

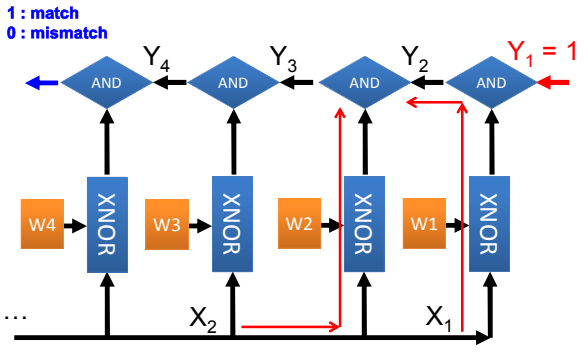

Figure 5. The "space" between two adjacent input bits. Red arrows show the traveling paths of two adjecant input bits within the same time period.

In other words, two different data streams could share the array hardware, assuming that one would want to search for the same pattern in each. Interleaved dataflow would allow for full hardware usage and the highest possible throughput.

V. Conslusion

New nanoelectronic devices have many design constraints, which make "copying" CMOS circuitry difficult. The design of a large-scale, useful non-CMOS nanoelectronic architecture for general-purpose computing carries many challenges. This motivated our work to demonstrate a scalable nanoelectronic circuit for special-purpose computation (pattern matching).

We demonstrated the design of an NML systolic pattern matching circuit from out-of-plane nanomagnets and thoroughly discussed the information flow and the time constrains in this structure. The device contains 23 nanomagnets per tile, operated by a homogenous, oscillating magnetic field and in principle, an arbitrary number of tiles can be used to match long patterns. We believe that this structure is experimentally feasible and experimental realization is ongoing.

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