Modeling Random Dopant Fluctuation Effects in Nanoscale Tri-Gate MOSFETs

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INTRODUCTION

The tri-gate FET has been hailed as the biggest breakthrough in transistor technology in the last 20 years. The increase in device performance (faster switching, low power, improved short channel effects, etc.), coupled with the reduction in device size, would allow for huge gains in the electronics industry [1]. In this work, we investigate the performance of the tri-gate FET when compared to the planar counterpart, and show how quantum size quantization and random dopant fluctuations (RDF) affect the tri-gate FET performance and how to curb these issues.

SIMULATION MODEL

A 3-D fully *atomistic* quantum-corrected Monte Carlo device simulator has been used in this work. Quantum mechanical space-quantization effects have been accounted for via a *parameter-free* effective potential scheme [2] and benchmarked against the NEGF approach in the ballistic limit [3]. To treat full Coulomb (electron-ion and electron-electron) interactions properly, the simulator implements two real-space molecular dynamics (MD) schemes: the particle-particle-particle-mesh (P^3M) method and the corrected Coulomb approach. The essential bandstructure parameters (bandgap, effective masses, and the density-of-states) have been computed using a 20-band nearest-neighbour $sp^3d^5s^*$ tight-binding scheme.

DISCUSSION

The dimensions of the devices being simulated are as follows (unless otherwise stated): $T_{OX} = 2$nm; n^+ polysilicon gate material; $L_{CH} = 18$nm; $N_A = 2\times10^{18}$ cm^{-3}; $W = 10$nm; S/D contact length = 31 nm; S/D junction depth = 15nm; S/D doping density = 5×10^{19} cm^{-3}; Ohmic S/D contact; technology node voltage, $V_{DD} = 0.8$V.

Looking at Fig. 1 we can see both the planer and the tri-gate transistors experience some fluctuation in threshold voltage due to *randomness in the channel* region, but this deviation is smaller (~22mV) in the tri-gate. Also, threshold voltage is much smaller for the tri-gate FET. However, we see that when we perform the same simulation with random dopants in the S/D region the effects become very prominent. Fig. 2 shows the percentage deviation for both devices is much larger than in either of the previous simulations, but we again see a much *smaller* deviation in the tri-gate device (25%) when compared to its planar counterpart (102%).

Next, a variety of methods were implemented to limit the RDF, with the goal to decrease the percent deviation and still maintain an acceptable level of on current. Figs. 3-6 show the variation of ON current as a function of channel doping density, S/D doping density, S/D workfunction, and S/D junction depth. Of all these, in Fig. 6, we see an increase in drive current as junction depth increases because of the decrease in resistance in both regions. Also noticeable is that as we increase the junction depth we see a decline in drive current variation.

CONCLUSION

The main findings are as follow: 1) carrier scattering in a tri-gate FET leads to ON current degradation of ~30% and hence cannot be ignored; 2) RDF is smaller in the tri-gate FET; 3) RDF due to the S/D discreteness can be engineered by adjusting the S/D junction depth.

ACKNOWLEDGEMENT

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[2] S. Ahmed, C. Ringhofer, D. Vasileska, "Parameter-Free Effective Potential Method for Use in Particle-Based Device Simulations," *IEEE Trans. on Nano.*, 4, pp. 465–471, 2005.
[3] *nanowire* simulator at http://nanohub.org/tools/nanowire/

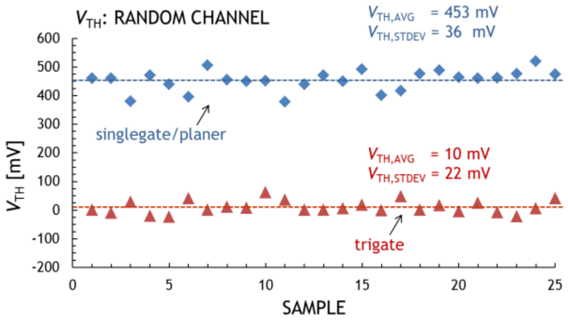

Fig. 1. V_{TH} comparison with random channel dopants.

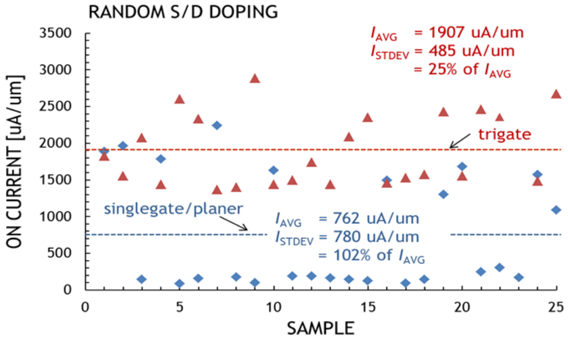

Fig. 2. I_{ON} comparison with random source/drain doping.

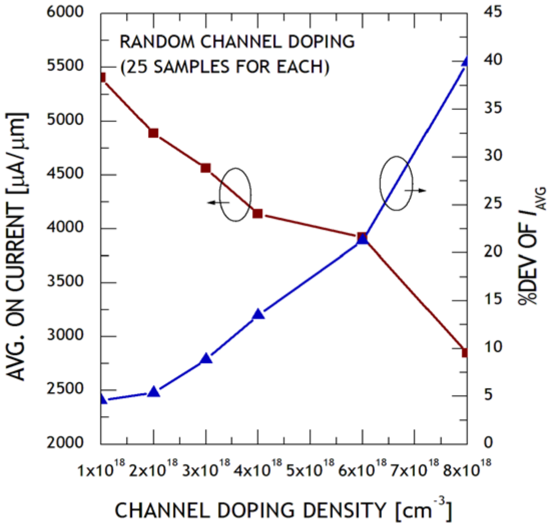

Fig. 3. RDF as a function of channel doping density.

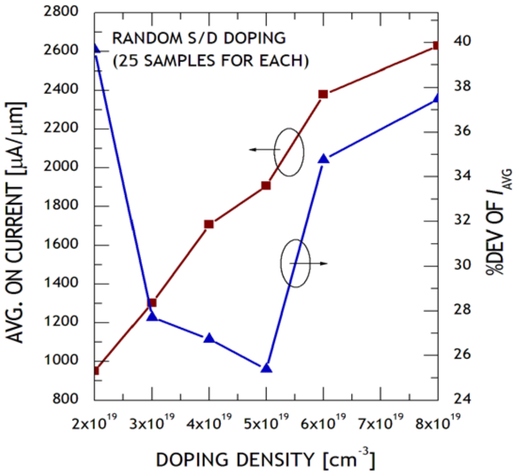

Fig. 4. RDF as a function of source/drain doping density.

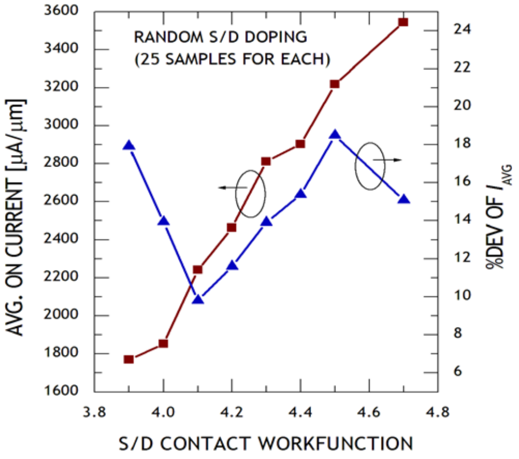

Fig. 5. RDF as a function of S/D contact workfunction.

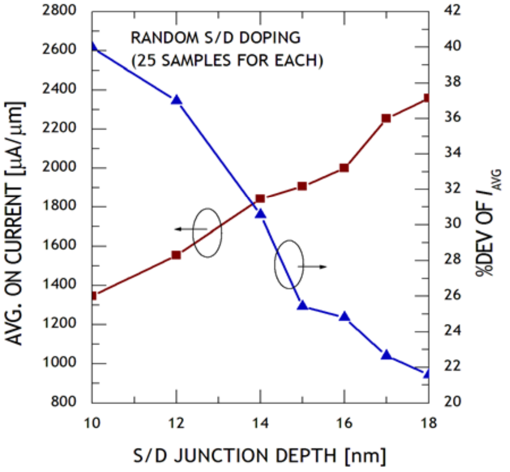

Fig. 6. RDF as a function of source/drain junction depth.