# Design of a Systolic Pattern Matcher for Nanomagnet Logic

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## Introduction: Systolic Computing Structure With Nanomagnetic Logic

Systolic computing arrays are highly parallel processors operating on data streams. They have a regular matrix-like structure [1]. Their regular layout naturally lends itself to nano-scale implementations. Nanomagnet Logic (NML) is emerging as a promising candidate for "beyond-CMOS" computing devices [2]. So far only relatively simple circuits were designed in NML. This paper presents an NML-based systolic pattern matcher that is in principle scalable to an arbitrarily large circuit.

## Computation Model of NML Computing with Global Clocking

Partially irradiated Co/Pt multilayer nanomagnets were shown to have non-reciprocal coupling, resulting in well-controlled signal flow and error-free computing [3]. They are inherently pipelined on the bit level. The layout of a XOR gate consisting of several gates is illustrated in Fig. 1.

A global oscillating field is needed to clock the NML system. The amplitude of the clocking field can be as low as 10 mT, enabling low-power operation.

Object Oriented MicroMagnetic Framework (OOMMF) and Matlab-based pre-processor package are used as our micromagnetic simulation tools [4]. The point-wise changing parameters are calibrated by fitting with experimental data [3].

## Structure of Systolic Pattern Matcher

Systolic architectures are built from cascaded data processor units (DPU). Every DPU computes simultaneously and only neighbouring DPUs communicate (see Fig. 2). Systolic pattern matcher is used to find a pre-defined pattern in an incoming data stream. The structure of one single unit used for pattern matching is given in Fig. 3, where one XNOR gate and one AND gate are employed for 1-bit pattern matching. Our designed layout with nanomagnets is presented in Fig. 4. An N-bit (N = 2, 3, 4…) systolic pattern matcher can be built by connecting N units. The signal flow is described in detail in Fig. 5, where the input data stream and output data stream are propagating in different directions.

The parameters of the micromagnetic simulations are calibrated by fitting experimental hysteresis curves.

## Results

We designed and simulated an NML-based systolic pattern matcher. The footprint for each DPU is 1 μm by 650 nm. Our simulation verified that with a proper clocking, the functionality of an N-bit systolic pattern matcher can be achieved and the working frequency can be up to a few tens of MHz. The switching of a single nanomagnet with the given size of 100 nm by 100 nm dissipates energy of 715 $k_BT$, which can be lowered by shrinking the magnet size.

## Acknowledgement

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## References

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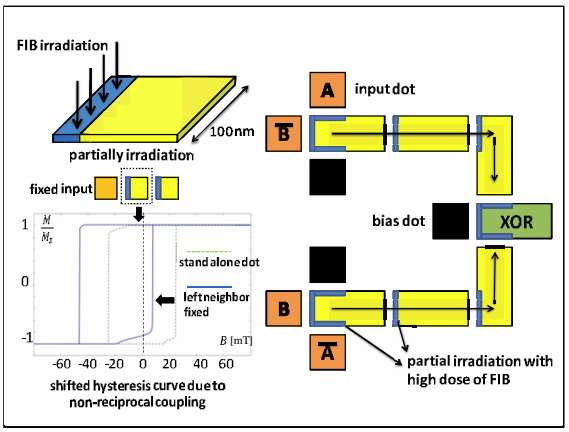


Fig. 1. Due to the partial Focused Ion Beam irradiation (blue region), switching always starts at the irradiation side, which can be exploited to one-directional information flow. This structure demonstrates the design for a XOR gate: Black dots are bias dots deciding whether the majority gates work as a AND gate or OR gate.

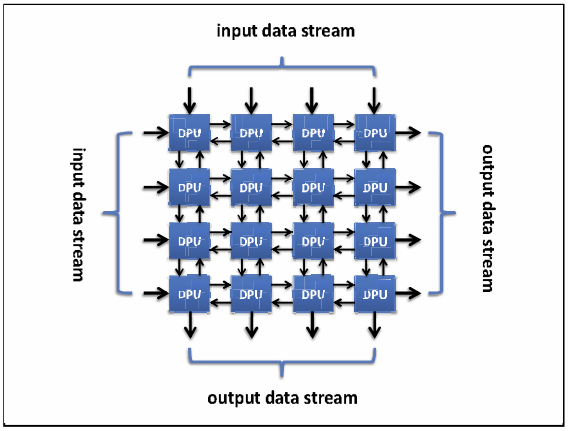


Fig. 2. Structure of generic systolic array: communication only exists between neighboring DPUs, and only the DPUs at the border can communicate with outside. Information streams can flow to different directions.

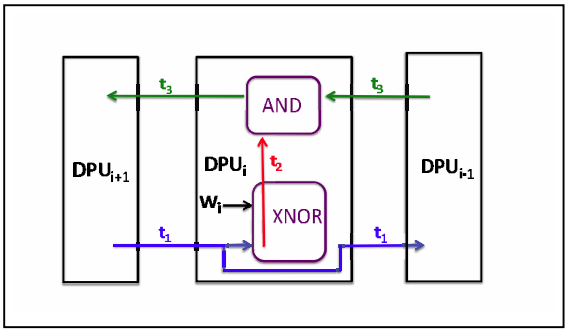


Fig. 3. Information flow in systolic pattern matcher: each DPU consists of one XNOR gate and one AND gate. t1, t2 and t3 are the consumed time for each DPU to receive, compute and send data respectively. Input data stream comes in from the left bottom, and is transferred from left to right one DPU after another; the output data stream propagates from right to left.

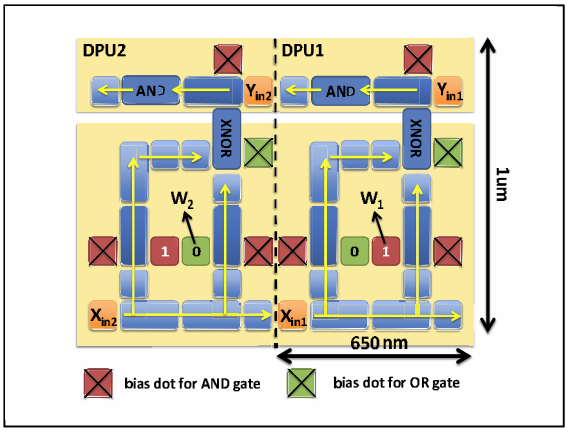


Fig. 4. The sketch of a layout for a two-bit systolic pattern matcher: the yellow arrows show information flow in the structure. The bits of pattern are saved stably in dots W1 and W2. The data stream to match with W1 and W2 comes in from the left bottom and the final output comes out from the left top. Two DPUs can be connected directly without adding extra dots in between. The footprint of one DPU in our simulation is 1 μm by 650 nm.

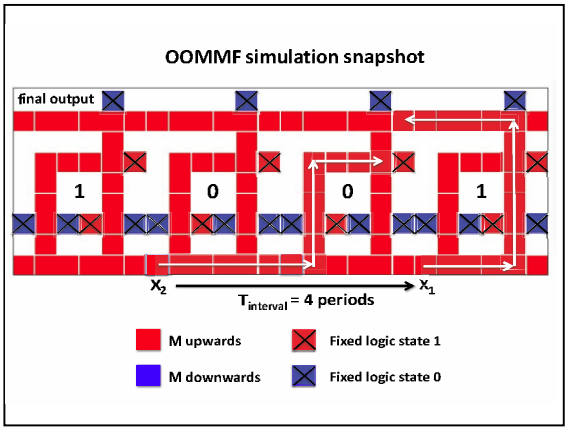


Fig. 5. The snapshot of a 4-bit systolic pattern matcher from OOMMF simulation: data step forward two dots after each period of oscillating field. Propagation time has to be considered during designing the layout in order to make sure the two data from different paths can meet correctly. One period of external clocking field in our simulation is 15 nanoseconds. The sizes of square dot and elongate dot are 100 nm by 100 nm and 210 nm by 100 nm respectively, and the distance between two neighbors is 10 nm. The amplitude of oscillating field is 52 mT, which can be reduced to around 10 mT to be more power-efficient.