Diffusion based Memristor Compact Model

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Piecewise linear, calculus and behavioral PSPICE memristor models are readily available in literature [1-2]. We present a PSPICE compatible, scalable, closed form compact memristor model.

Defects or vacancies in the nano-film serving as body of memristor, drift with applied voltage (v) as in Fig. 1. The continuity equation without generation (G) and recombination (R) terms, with initial conditions u(x,0) = $\alpha/(1+\alpha)$ and final constraints u(0,∞) = 0, u(d,∞) = 1, was used to derive temporal evolution of defect concentration u(x,t), where α is the ratio of defect to ideal ion-concentrations (a/(1-a)) in the chemical species, known from the manufacturing recipe (1).

$$u(x,t) = \frac{\alpha\, e^{\left(f_0\,\phi + \frac{1}{fx\,\phi}\right)}}{1+\alpha\, e^{\left(f_0\,\phi + \frac{1}{fx\,\phi}\right)}} \qquad (1)$$

Formulating the resistance r(t) = $\gamma/((1+\eta)-u(x,t))$ allows us to model a finite min and max resistance, which for $\eta \to 0$ simplifies to (2), where η prevents computational singularity.

$$r(t) = \gamma\left(1 + \alpha\, e^{\frac{1}{1+\alpha}}\, e^{f_0\phi}\right) \qquad (2)$$

In (2), γ is the experimentally determined lowest memristor resistance. The natural frequency $f_0 = \mu/d^2$, where μ is defect mobility and d is device length. For x in $f_x = \mu/(x \cdot d)$, eqn.(2) uses the location at which accumulation of defects occurs, as in Fig. 1. Parameter ϕ is the flux (time integral of voltage) that accumulates with applied voltage. An IV curve produced from this formula is in Fig. 2. Cycles 1, 2 produce symmetric lobes. Cycle 3 backtracks cycle 2 and cycle 4 drives the device to a higher resistance. A simplified switching time formula derived from (2) is given below and equivalent, for the $\log_e$ term equal unity, to [3].

$$tt = \frac{d^2}{v\,\mu}\ln\big((1+\alpha)(rr - 1/(1+\alpha))\big) \qquad (3)$$

Fig. 3(a) shows timing contours proportional to resistance ratio (rr) for a fixed defect concentration (a), as expected. Fig. 3(b) shows alpha contours that satisfy a combination of switching time (tt) and resistance ratio.

For integration into a circuit design environment, we represent the memristor as a two terminal device in PSPICE simulator. This implementation is summarized in the block diagram in Fig. 4 and is based on existing fundamental PSPICE elements. The applied voltage across the device is computed using the summer U1, converted by U2 to a current and computed as in (2), using U3 – U6. U3 is a trans-conductor. U4 generates flux as the voltage across a capacitor, by integrating current from U2. The exponential current is realized via an ideal diode, with the flux (voltage) applied across it [4]. Constant and variable currents are summed in U5, converted to voltage in U6 and drive a voltage-controlled resistor, U7. For comparison, in Fig. 5 we overlay the IV curve, from the analytical model above with the PSPICE implementation. All plots use $\alpha = 1$, $\mu = 10^{-13}m^2/Vs$ and $\gamma = 10^3\Omega$.

Our model exhibits known quasi-static memristor behavior and matches published switching time. The model can easily be ported to commercial simulators (PSPICE). The IV curves in Fig. 6 indicate that resistance is proportional to defect concentration for a fixed frequency and Fig. 7 shows that the device IV tends to a straight line for increasing frequency, both as expected.

This PSPICE compatible compact model for the memristor is backed by derivation from the continuity PDE. The model generates good quality, diverse simulation data in spite of approximations such as the fixed accumulation boundary, lack of statistical sophistication and the 1-D nature of the model.

REFERENCES

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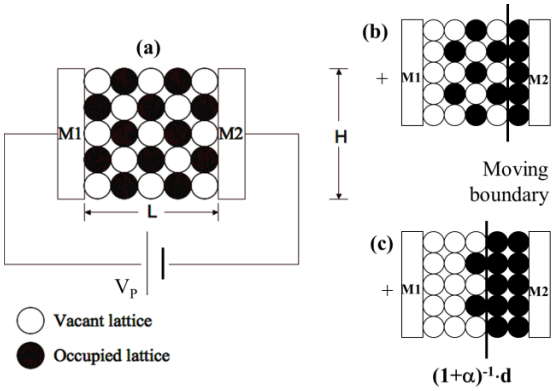

Fig. 1. The simple 1D memristor model. The accumulation boundary is mobile, but approximated as static in this paper.

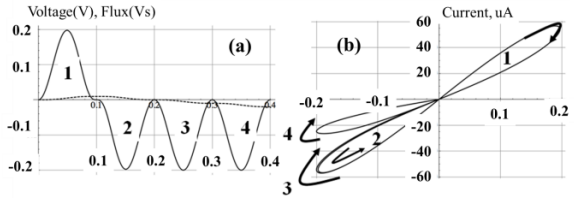

Fig. 2. The forcing sinusoid (bold) and flux (dotted) are shown in inset (a). Inset (b) shows the IV curve. During sinusoid cycle 1, the device traces out a low-to-high resistance path, then returns to the origin along the lobe 2 for cycle 2. During cycles 3 and 4, the device is forced into successive higher resistance states.

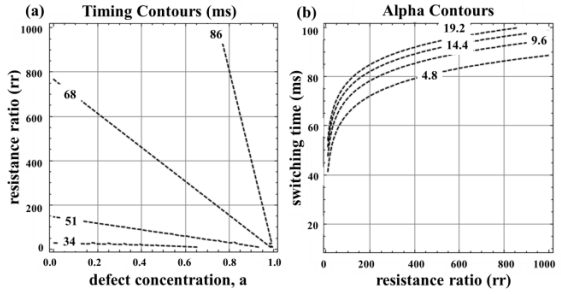

Fig.3. Contour plots for switching time, inset (a) and alpha, inset (b).

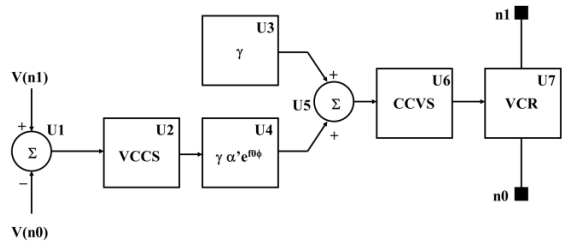

Fig.4. Block diagram showing PSPICE implementation.

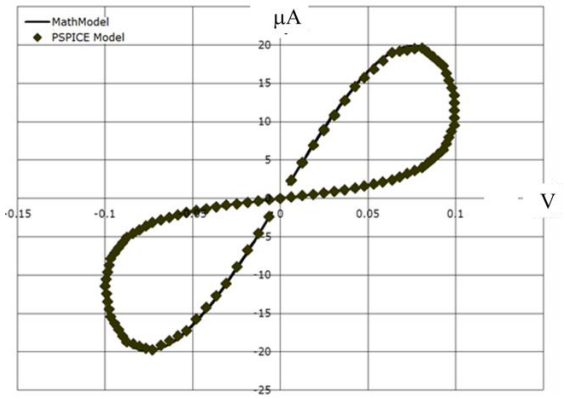

Fig. 5. Overlay of PSPICE and mathematical IV curves.

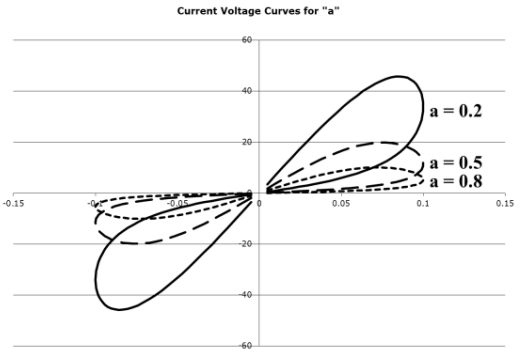

Fig. 6. IV curves for various defect concentration ratio a.

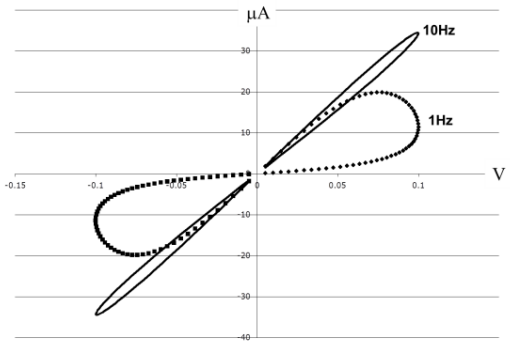

Fig. 7. IV curve lobes become thinner for higher frequency of excitation.