

Parallel Simulation of Nanowire Field-Effect Transistors

S. Baumgartner*, M. Vasicek*, and C. Heitzinger*[†]

*Wolfgang Pauli Institute c/o Department of Mathematics, University of Vienna, Austria.

[†]Department of Applied Mathematics and Theoretical Physics (DAMTP), University of Cambridge, UK.
e-mail: stefan.baumgartner@univie.ac.at

INTRODUCTION

Nanowire field-effect transistors (NWFETs) are attractive sensing devices for bio- and gas molecules with a wide range of applications [1], [2]. The working principle is the following: the field-effect induced by target molecules at the sensor surface modulates the conductance of semiconducting nanowires consisting of silicon, SnO_2 , or other materials. The simulation of NWFETs is challenging due to the inherent multiscale problem, high aspect ratios, and large linear systems. These challenges can be overcome by the parallelization technique presented here. It is—of course—applicable to all kinds of semiconductor devices in addition to the structures considered as leading examples here.

MODEL AND PARALLELIZATION

Three material dependent PDEs are used for the simulation of charge transport and hence the sensing mechanism in NWFET devices (see Fig. 1). The charges and screening outside of the transducer are described by the Poisson-Boltzmann equation. In a boundary layer around the surface of the sensor, the charges responsible for the field-effect can be modeled by microscopic, macroscopic, or empirical methods. They are self-consistently coupled to the Poisson equation by a homogenization result [3].

The nanowire sensor itself is governed by the drift-diffusion-Poisson system [4], [5]. We proved existence and local uniqueness around thermal equilibrium for a solution of this system in [6] for bio- and gas sensors.

For engineering applications it is crucial to use an efficient parallelization technique capable to solve the drift-diffusion-Poisson system with jump conditions originating from the homogenization method. Therefore we developed a novel finite element and

tearing interconnecting (FETI) method, where the jump conditions are inherently included.

Here the simulation domain for the electrostatic potential and the charge carriers is split into blocks and is reconnected by Lagrange multipliers.

RESULTS

The electrostatic potential of the sensor and the electron density of an n-doped nanowire are presented in Fig. 2 and Fig. 3, where the different blocks of the parallelization technique are also indicated. Here the z -direction is divided in only two blocks. The electrostatic potential of the NWFET device is depicted in Fig. 4.

In Figs. 5 and 6, the same device is simulated with four blocks in the z -direction. The solution is identical, verifying the correctness of our method.

CONCLUSION

The novel FETI method presented here is applicable to all devices simulated by the drift-diffusion-Poisson system even containing discontinuities in the solution and its normal derivative at interfaces.

Parallel simulation allow us to speed up simulation on modern hardware and to calculate solutions on very large grids, since each node only has to store part of the grid.

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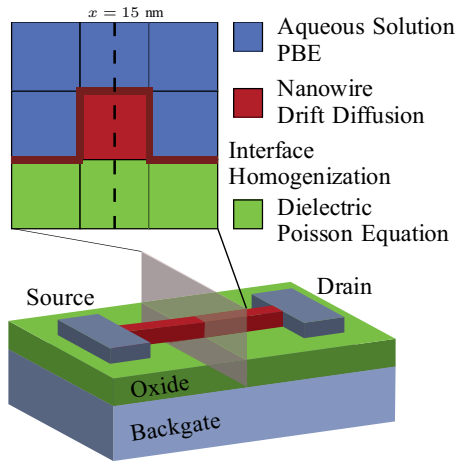


Fig. 1. Schematic diagram of the NWFET device. The different equations used in the simulations and the cross section $x = 15$ used in the remaining figures are indicated. The blocks for parallelization have a size of $10 \times 10 \times 10 \text{ nm}^3$ (Fig. 2, 3) or $10 \times 10 \times 5 \text{ nm}^3$ (Fig. 4, 5, 6).

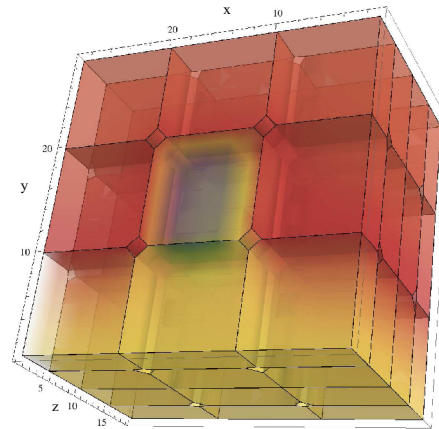


Fig. 4. Electrostatic potential of an n-doped NWFET device with a minimum potential of -0.0385 V (blue) and a maximum potential of 0.0066 V (red) in the 36 blocks of the parallel computation.

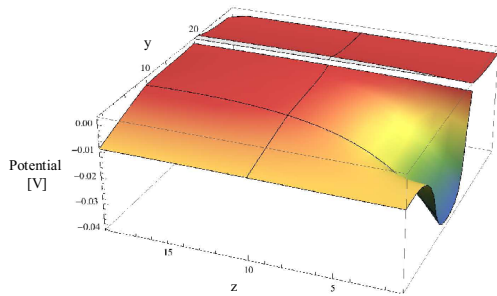


Fig. 2. The electrostatic potential at $x = 15 \text{ nm}$. The jump of the potential due to the homogenization method is clearly visible at $y = 20 \text{ nm}$.

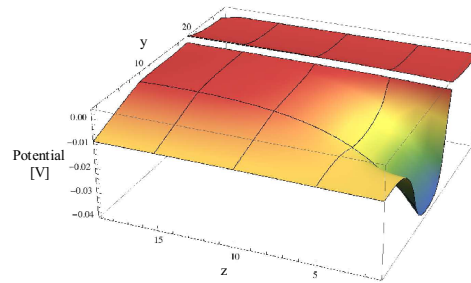


Fig. 5. The electrostatic potential at $x = 15 \text{ nm}$ as in Fig. 2. Here 4 blocks in z -direction have been used for parallelization.

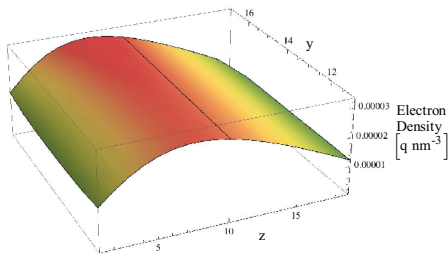


Fig. 3. Cross section of the electron density at $x = 15 \text{ nm}$. The electron density is computed on two blocks due to the splitting of the z -coordinate for the parallelization.

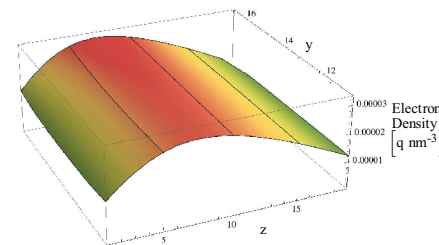


Fig. 6. Cross section of the electron density at $x = 15 \text{ nm}$ as in Fig. 3. Here 4 blocks in z -direction have been used for parallelization.

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