Full-band self-consistent modeling study of the electrostatics in FDSOI technology

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INTRODUCTION

CMOS technology development in industry requires the performances of novel technological boosters, as High-K dielectrics, substrate orientation and mechanical strain to be evaluated and modeled. Their effects on electrostatics, channel mobility and gate leakage have to be clearly quantified [1]. Fully-Depleted Silicon On Insulator (FDSOI) technology has been proven to be a promising candidate for nanoscale nodes. In this paper, we discuss a self-consistent modelling methodology based on a Poisson- k.p-Schrödinger (PS) model. The effects of band structure models, quantum confinement, mechanical strain, and substrate orientation on device electrostatics are analyzed and applied to analyse FDSOI technology.

MODELS AND DEVICE ELECTROSTATICS

In technology development, a rigorous modelling approach requires investigating the approximations introduced in conventional TCAD and analytical models to verify their accuracy. Within these perspectives, we present self-consistent 1D Poisson-k.p-Schrödinger simulations obtained using various state of the art band structure models. For electrons we have compared the predictions obtained with the recent 2-band k.p model [2] to the ones of the widely used effective mass approximation as well as the ones of the full band 15-levels k.p [3] and $sp^3d^5s^*$ Tight-binding [4] models. In all cases, a dense meshing in reciprocal space is considered for accurate quantum charge calculation as depicted in Fig. 1. Similar comparisons have been performed for holes with 6-bands k.p model [5].

NFET and PFET devices have been integrated in an FDSOI technology and characterized with AC capacitance measurements. The process includes High-K-Metal gate dielectric stacks with variable thickness (1.8 nm for HfO_2 and 1.1-3.9 nm for the interfacial dielectric). Figure 2 illustrates measurement and simulation results performed on all the considered CMOS devices where the dielectric physical thicknesses measured from transmission electron microscope characterization have been applied. Two-band and 6-band k.p model results for e^- and h^+, respectively, have been shown to match electrical characteristics with the same set of model parameters for all the devices. Figure 3 more clearly demonstrates the model capabilities in the evaluation of quantum effects when wafer orientation and Si layer thickness is varied. The two-band approach guarantees good predictions without sacrificing computational speed as in the e.g. full band 15-band k.p model. The minimal dependence of the CV characteristics on wafer orientation or band structure model indicates that the extension of the dark space is marginally affected by them. This is even more evident in Figure 4, where the results on the thin-oxide PFET device with a simpler Effective Mass Approximation model (EMA) and the 6-band k.p for h+ are compared.

DENSITY OF STATES

An accurate description of the Density Of States (DOS) is key features for accurate carrier density modelling within a realistic transport model. Indeed, the DOS not only depends on the band energies but also on their gradient with respect to wave vector. The electron DOS calculated with EMA at V_G=0V and 1V in the NFET device has been compared with the 2-band and 15-band model results (Figure 5). In the two former models, Δ- electrons are treated individually (red and blue curves). Also in this case, spurious divergences of the DOS can occur in multi-band models due to band crossing. Electron DOS has been calculated also for the [110] and [111] wafer orientations (Figure 6 (left)). This promotes illustrates how the 2-band k.p model represents. The validity of the model is confirmed in Figure 7 (right), where the DOS computed for [111] orientation for the three Δ valleys. Due to the warping of the valence bands, the DOS calculated with EMA is significantly different to the one obtained with 6-bands k.p model as depicted in Fig. 7.

CONCLUSION

By comparing several band structure models we have been able to illustrate the tradeoffs involved in modelling device electrostatics and density of states in FDSOI cutting-edge technology. The comparison indicated that a combination of 2-band k.p model for e- and 6-band k.p model for h+ represents an excellent compromise between the accuracy of full-band models (e.g. 15-band k.p) and the low computational effort of EMA approaches. These self-consistent models have been used for the analysis of mobility vs. wafer orientation or mechanical strain and further results will be discussed at the IWCE 2012 conference.

REFERENCES

[1] ITRS http://www.itrs.net/reports.html
[2] O. Baumgarten, et al., SSE 54, 143 (2010)
[3] D. Rideau, et al., PRB 74, 195208 (2006)
[4] Y.M. Niquet, et al., PRB 79, 245201 (2009)
[5] M.V. Fischetti, et al., JAP 94, 1079 (2003)

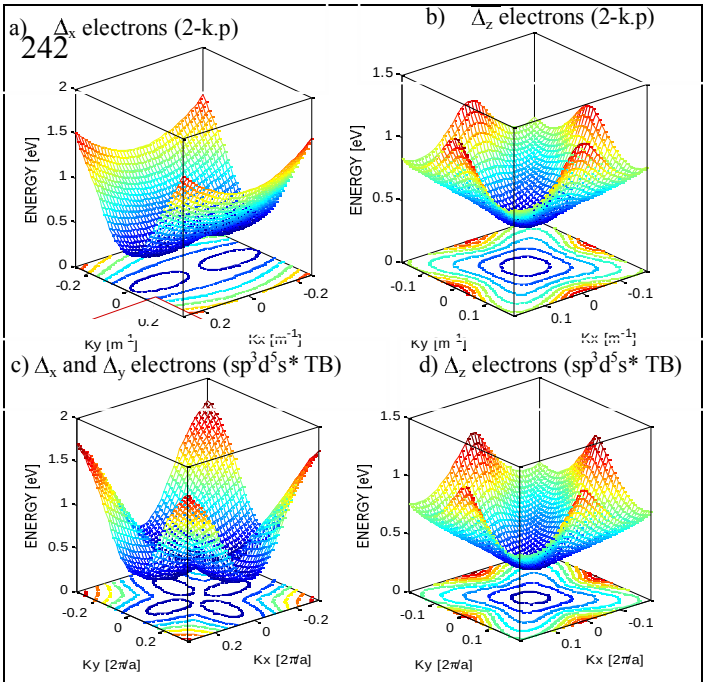

Fig. 1. Si electron band structure in Δx (a,c) and Δz (b,d) valleys using the 2-band (a, b) and full bands (c, d) $sp^3d^5s^*$ TB models.

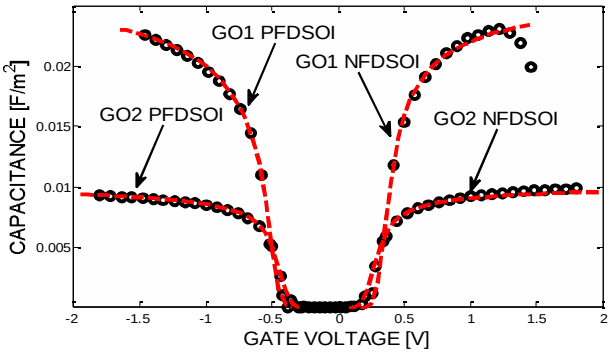

Fig. 2. Gate capacitance vs. voltage results (measurements - symbols - and model - lines) for thin (GO1 – T_{ox} = 1.8+1.1 nm) and thick (GO2 – T_{ox} = 1.8 + 3.9 nm) oxide PFET and NFET FDSOI. Results have been obtained with PS simulations with meshing in k space, with a 2-band model for e- and a 6-band k.p model for h+.

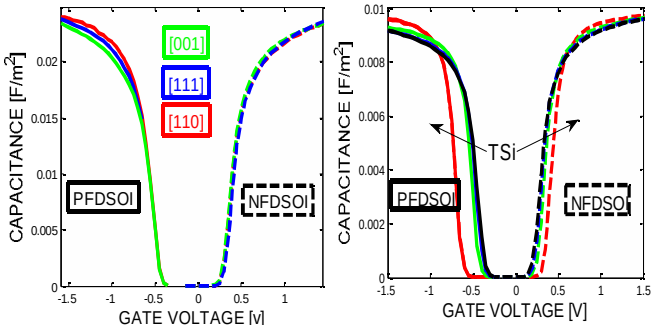

Fig. 3. Gate capacitance vs. voltage curves simulated for different wafer orientations and Si layer thicknesses T_{si} variations (2-8nm).

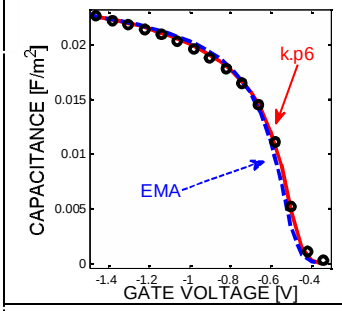

Fig. 4. Measurements (symbols) vs. model (lines) of gate capacitance on GO1 PFET FDSOI [100] device. EMA models have been calibrated to match full band simulations results with meshing in k space.

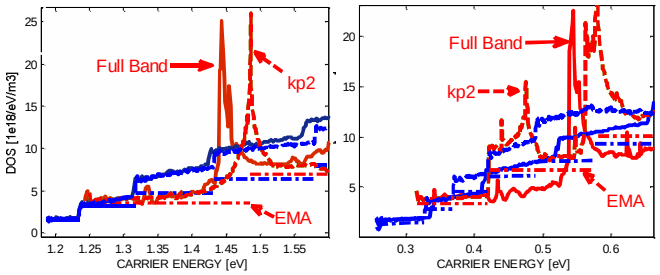

Fig. 5. Electron DOS per valley vs. carrier energy in unbiased (left) and at VG=1V (right) NFET (TSi=5nm) calculated with EMA (dashed dot lines), 2-band k.p (dashed lines), and full band model (lines). Red curves refer to Δx, Δy valleys that are doubled, while blue curves are related to Δz valleys.

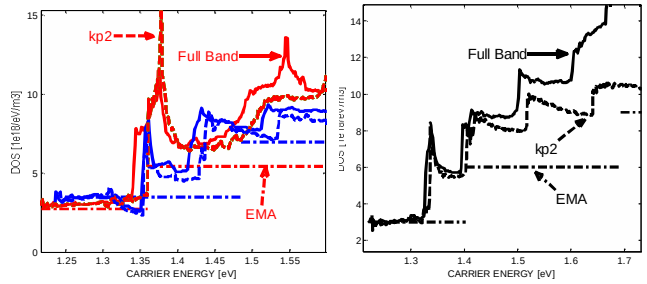

Fig. 6. (Left) Same plots as in Fig 5, but for [110] and [111] directions. (Right) For [111] orientation the DOS from the 3 valleys are equivalent.

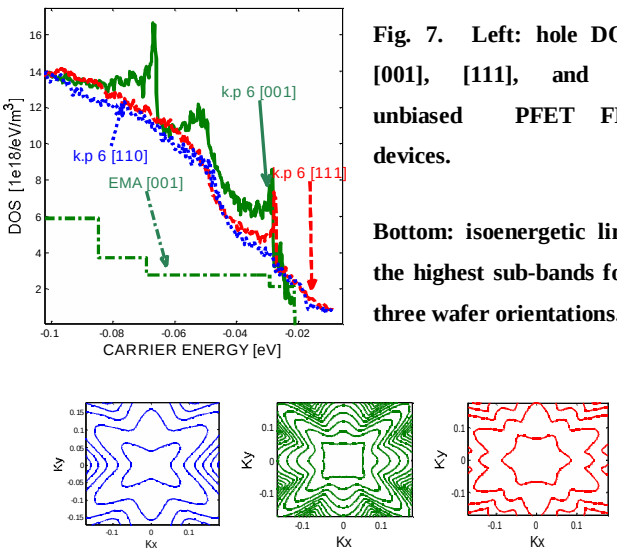

Fig. 7. Left: hole DOS in [001], [111], and [110] unbiased PFET FDSOI devices.

Bottom: isoenergetic lines of the highest sub-bands for the three wafer orientations.