Study of the Role of Different Phonon Scattering Mechanisms on the Performance of a GAA Silicon Nanowire Transistor

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The Gate-All-Around Nanowire transistor (GAA NWT) architecture offers the best electrostatic integrity and therefore is a strong candidate to replace the traditional planar bulk MOSFETs for CMOS applications at the end of the road-map [1]. Even though, at small channel lengths, electron transport was expected to be ballistic, it has been shown that for small NWT cross-sections the electron-phonon interaction increases and plays a major role in mobility degradation [2], [3]. Additionally, from a physical point of view, phonon scattering is the main source of de-coherence and energy relaxation in electron transport. Understanding the role of the different phonon mechanisms is important for TCAD applications in which accuracy as well as speed are paramount. Neglecting unimportant mechanisms can potentially save computational time. Recent works have carried out studies of the role of different phonons in nanowires [4], [5], but did not study comprehensively the role of the bias, and hence the barrier shape on their impact on the transfer characteristics. In this paper, we investigate the impact of the different phonon scattering mechanisms on the performance of a Silicon GAA NWT using the Non-Equilibrium Green's Function (NEGF) formalism to describe the electron quantum transport in the device.

The quantum carrier transport is described using the NEGF approach, using an effective-mass Hamiltonian. The effective masses were extracted from Tight Binding calculations to capture the dependence of the electron band structure on the nanowire diameter. Phonon scattering is included in the self-consistent Born approximation considering bulk phonon parameters as described in [3]. Three types of f- and g- optical phonons are considered, which allow electron transitions between non-equivalent/equivalent valleys as shown in Fig. 1. Intravalley acoustic phonons in an elastic approximation are also included. The nanowire investigated in this work has a 2.2×2.2 nm^2 cross-section and a 20 nm channel length with an equivalent oxide thickness of 0.8 nm. The source and drain extensions are 15 nm long with a uniform doping concentration of 10^{20} cm^{-3}.

The transfer characteristics for the nanowire transistor are shown in Figs. 2 and 3 for drain biases of $V_D = 1$ mV and $V_D = 0.6$ V, respectively. The $I_D - V_G$ for the ballistic transistor (B), the device with all phonon scatterings included (S), the device with only acoustic phonons (A) included, the device with only g-type phonons (G), and the device with only f-type phonons (F) are shown.

Figs. 4 and 5 show the drain current reduction defined as $(1 - I_{scat}/I_{ball})$ for both drain bias conditions. The results for the device (S) show a similar behaviour to that shown in [6], although the values of the reduction are slightly overestimated in our simulations. Acoustic phonon scattering is the main responsible for the reduction in the current at both bias conditions. This is clearly seen in Figs. 4 and 5, which show the drain current reduction defined as $(1 - I_{scat}/I_{ball})$ for both drain bias conditions. The relative impact of this mechanism decreases with increasing gate bias, but the role of intervalley optical phonons becomes more important. However, it is clear from the plots that there is a qualitative and quantitative difference in the dependence of the drain current reduction with the gate bias at low and high drain voltages.

The drain current reduction at low gate voltages is similar in both situations and is dominated by acoustic phonon scattering. However, at $V_G = 0.9$ V and $V_D = 1$ mV acoustic phonons produce a 75% lowering of the current, whereas at $V_D = 0.6$ V the drain current reduction for (A) drops to 50%.

The extracted resistances at $V_D = 1$ mV and $V_G = 0.9$ V for (S), (A), (G) and (F) are 5.39×10^4, 3.32×10^4, 1.15×10^4, and 2.7×10^3 Ω, respectively. The resistance obtained from adding the devices (A), (G) and (F) is equal to 4.74×10^4 Ω. This value is 12% lower than the value obtained for the device (S), which indicates that the Matthiessen's rule is violated in these nanoscale devices as already shown previously through semi-classical simulations [7], [8].

ACKNOWLEDGMENT

M.A. thanks the Xunta de Galicia for the awarded Angeles Alvariño fellowship and for the visiting fellowship in the College of Engineering, Swansea University,

co-funded by the Fondo Social Europeo (FSE). A.M. has been supported by an EPSRC Career Acceleration Fellowship, EP/I004084/1.

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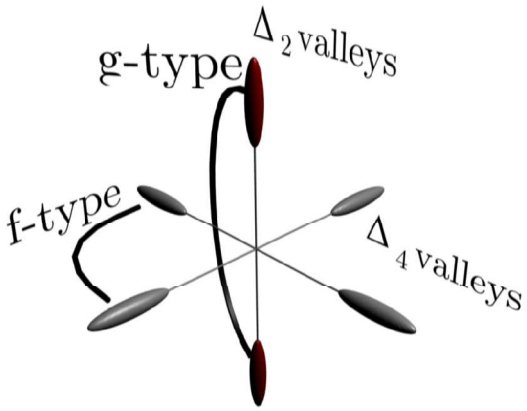

Fig. 1. Schematic of intervally phonon-mediated transitions between the Δ valley minima in silicon.

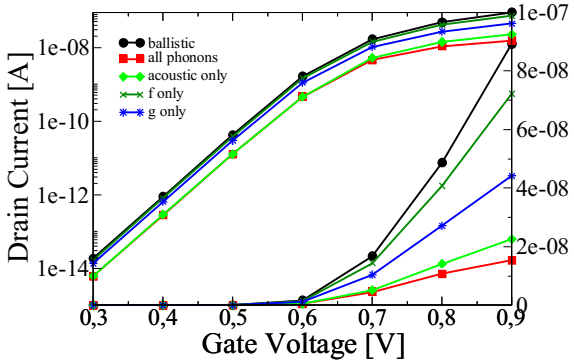

Fig. 2. The $I_D - V_G$ characteristics at $V_D = 1$ mV for the 20 nm gate length silicon nanowire transistor with the different phonon mechanisms in operation.

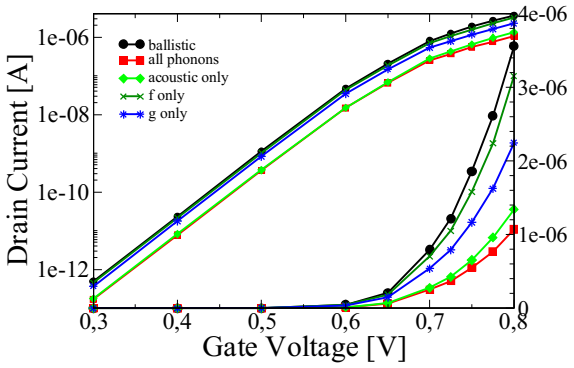

Fig. 3. The $I_D - V_G$ characteristics at $V_D = 0.6$ V for the 20 nm gate length silicon nanowire transistor with the different phonon mechanisms in operation.

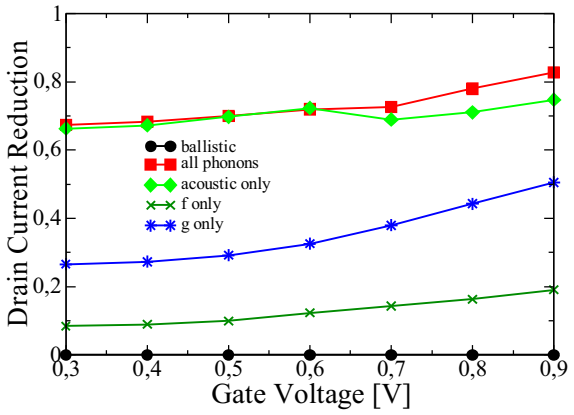

Fig. 4. Drain current reduction at $V_D = 1$ mV for the 20 nm gate length silicon nanowire transistor with the different phonon mechanisms in operation.

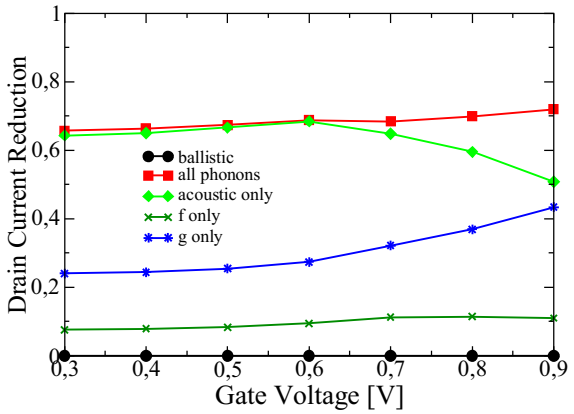

Fig. 5. Drain current reduction at $V_D = 0.6$ V for the 20 nm gate length silicon nanowire transistor with the different phonon mechanisms in operation.