Monte Carlo simulations of inverse channel versus implant free $In_{0.3}Ga_{0.7}As$ MOSFETs

K. Kalna[1] and J. S. Ayubi-Moak[2]
[1]College Of Engineering, Swansea University, Swansea SA2 8PP, Wales, UK
[2]Synopsys, Inc., Mountain View, CA, USA
e-mail: k.kalna@swansea.ac.uk

The introduction of higher mobility materials such as Ge [1] for *p*-type MOSFETs and III-Vs [2] for *n*-type MOSFETs for sub-16 nm technology is an accepted option. Surface channel (SC) III-V MOSFETs might struggle to take advantage of low effective mass and high injection velocity into the channel. Therefore, new device ultra-thin body concepts including an enhancement mode MOSFET with implant free (IF) source/drain regions [3] as well as HEMT structures [4] have been studied.

In this work, we compare the performance of two *n*-type III-V MOSFET $In_{0.3}Ga_{0.7}As$ channel architectures: (i) the SC design with implanted S/D (Fig. 1) and (ii) the δ-doped IF design (Fig. 2), each scaled to gate lengths of 35, 25 and 18 nm. The high-κ gate oxide is assumed to be GdGaO (GGO) with κ=20. The EOT is kept as close as possible in both SC and IF architectures during the scaling process. The doping profiles for the SC transistors are optimized using a drift-diffusion (DD) simulator (MEDICI). Conduction band profile and electron density in SC and IF MOSFETs are shown in Fig. 3, respectively.

This study is carried out using a hetero-structure finite element Monte Carlo device simulator MC/MOS [3,5] assisted by DD simulations. The main goal is to study the on-current including an electron (e) scattering with interface (soft) optical phonons (IP) [6]. The e-IP interaction is derived in a non-parabolic band-structure approximation, by calculating total (high/low frequency, $\varepsilon^{\alpha}_{TOT(f)}$ [α=∞,0]) dielectric functions via solving a biquadratic equation [Eq. (1)] considering the interface between dielectric (OX) and polar semiconductor (PS) which is then needed for a calculation of the interaction strength. Using the strongest TO phonon in GaO_2 with energy of 35.07 meV [7], we have found two interface TO phonons at the $GaO_2/In_{0.3}Ga_{0.7}As$ interface with energies of 29.85 meV and 52.52 meV, respectively. Fig. 4 shows the interaction strengths of the most important scattering mechanisms in the $In_{0.3}Ga_{0.7}As$ channel.

Fig. 5 compares subthreshold slope of the SC and IF $In_{0.3}Ga_{0.7}As$ MOSFETs when scaled to gate lengths of 35, 25 and 18 nm. Fig. 6 shows I_D-V_G characteristics at V_D of 1.0 V for 35, 25, and 18 nm gate length SC MOSFETs, respectively. The performance of equivalent gate length IF MOSFETs is shown in Fig. 7, at the same 1.0 V overdrive. Fig. 8 compares transconductance, while the average electron velocity in the scaled SC and IF devices is compared in Figs. 9 and 10, respectively, illustrating a much larger channel velocity in the scaled IF transistors. In summary, the SC transistor architecture suffers strongly from the IP scattering induced reduction in the on-current during the scaling when compared to the IF devices. However, the IF MOSFETs start to suffer from the IP scattering when channel thickness is reduced below 5 nm (not shown here). The SS of scaled transistors deteriorates similarly in the both SC and IF MOSFETs.

REFERENCES

[1] H. Shang et al., Electron Device Lett. 25, 135-137 (2004).
[2] R. Chau et al., IEEE Trans. Nanotechnol. 4, 153-158 (2005).
[3] K. Kalna et al., IEEE Trans. Nanotechnol. 6, 106-112 (2007).
[4] N. Waldron, D.-H. Kim, and J. A. del Alamo, IEDM Tech. Dig., 633-636 (2007).
[5] K. Kalna, L. Yang, and A. Asenov, Proc. ESSDERC, 169-172
[6] S. Q. Wang and G. D. Mahan, Phys. Rev. B 6, 4517-4524 (1972).
[7] Y.-M. Chang, L. Xu, and H. W. K. Tom, Phys. Rev. B 59, 12220-12223 (1999).

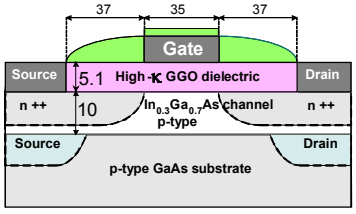

Fig. 1: Cross-section of the 35 nm gate length, *n*-type, surface channel (SC), $In_{0.3}Ga_{0.7}As$ MOSFET. Dimensions quoted in nm.

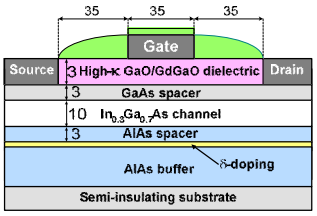

Fig. 2: Cross-section of the 35 nm gate length, implant free (IF) $In_{0.3}Ga_{0.7}As$ MOSFET. Dimensions quoted in nm.

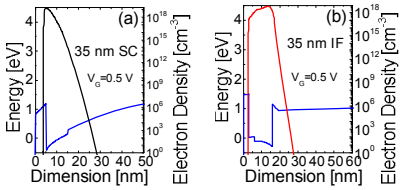

Fig. 3: Conduction band and electron density in the 35 nm gate length SC (a) and IF (b) MOSFETs.

$$\text{Eq.(1)}: \omega^4\left(\varepsilon_{OX}^{\infty}+\varepsilon_{PS}^{\infty}\right)-\omega^2\left[\varepsilon_{OX}^{0}\left(\omega_{OX}^{TO}\right)^2+\varepsilon_{OX}^{\infty}\left(\omega_{PS}^{TO}\right)^2+\varepsilon_{PS}^{0}\left(\omega_{PS}^{TO}\right)^2+\varepsilon_{PS}^{\infty}\left(\omega_{OX}^{TO}\right)^2\right]+\left(\omega_{PS}^{TO}\right)^2\left(\omega_{OX}^{TO}\right)^2\left(\varepsilon_{OX}^{0}+\varepsilon_{PS}^{0}\right)=0$$

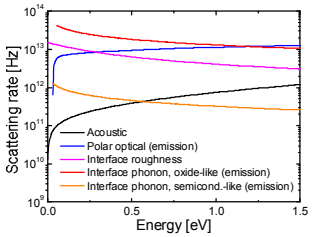

Fig. 4: Electron scattering rates vs. energy in $In_{0.3}Ga_{0.7}As$ channel.

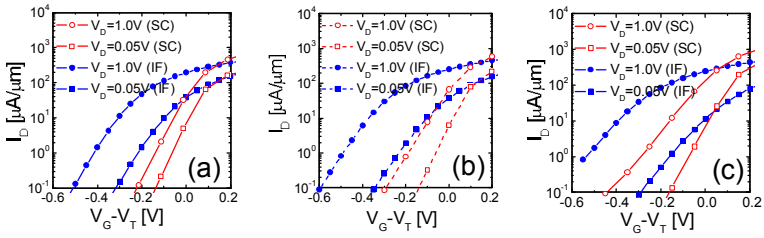

Fig 5: Subthreshold slopes at high and low V_D for 35 nm (a), 25 nm (b) and 18 nm (c) gate length SC and IF MOSFETs.

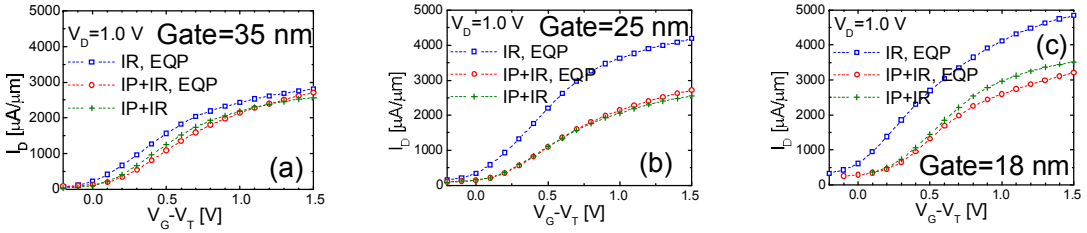

Fig. 6: I_D-V_G characteristics for the (a) 35 nm, (b) 25 nm and (c) 18 nm gate length SC $In_{0.3}Ga_{0.7}As$ MOSFETs at drain bias of 1.0 V, respectively. The incremental impact of interface roughness (IR), interface phonons (IP) and quantum corrections (EQP) used in MC simulations is also shown. The threshold voltage is adjusted to 0.0 V.

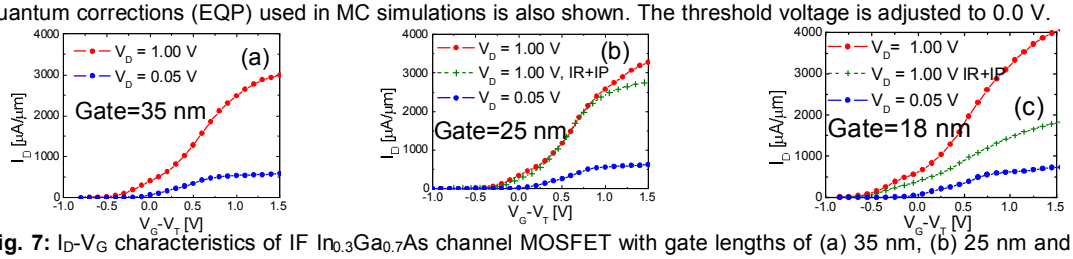

Fig. 7: I_D-V_G characteristics of IF $In_{0.3}Ga_{0.7}As$ channel MOSFET with gate lengths of (a) 35 nm, (b) 25 nm and (c) 18 nm at drain biases of 0.05 V and 1.0 V, respectively, showing the impact of interface roughness (IR) and interface phonons (IP). The quantum corrections (EQP) are always included and V_T is adjusted to 0.0 V.

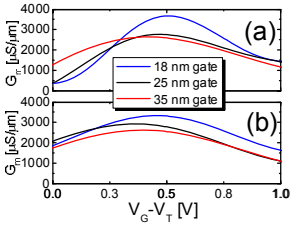

Fig. 8: Transconductance (G) for scaled SC (a) and IF (b) device architectures at V_D=1.0 V.

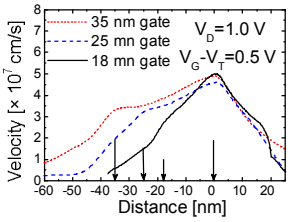

Fig. 9: Average velocity along the $In_{0.3}Ga_{0.7}As$ channel in scaled SC MOSFETs using IP, IR and EQP.

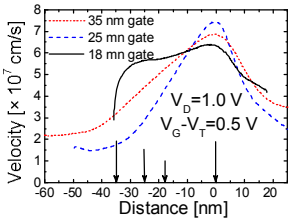

Fig. 10: Average velocity along the $In_{0.3}Ga_{0.7}As$ channel in scaled IF MOSFETs using IP, IR and EQP in simulations.