Parameter Optimization of NanoWire FET's using Taguchi method

S.P.Venu Madhava Rao* EVLN Ranga Charyulu** Dr.K.Lal Kishore ***
*SNIST,HYDERABAD email : spvenu@yahoo.com
**PJSMCET,HYDERABAD email:rangaevln@yahoo.com

***JAWAHAR LAL NEHRU TECHNOLOGICAL UNIVERSITY,HYDERABAD,INDIA

ABSTACT

The silicon nanowire (SiNW) transistors are considered as one of the most promising candidates for ultra-scaled low power logic and non-volatile memory applications due to their superior short channel controllability. nanowire (NW) transistors possess excellent scalability and performance. The near-ideal sub threshold slope and high drive current performance at low gate overdrive voltages make them ideal candidates for low power CMOS applications.

INTRODUCTION

silicon NanoWire MOSFET is fabricated on a bulk substrate with fully CMOS compatible technology. The epitaxially grown SiGe layer is served as a sacrificial layer to provide suspended NanoWire structure. The device shows excellent electrical characteristics. A body effect is effectively suppressed by the structure to cover all channel surfaces of the NanoWire. Moreover, capacitor less 1T-DRAM operation is approved due to the electrostatic floating body of such a device.

In a nanoscale CMOS era, various three-dimensional device structures: double-gate, tri-gate, □-gate, □-gate, and gate-all-around (GAA), have been explored to provide better gate to channel controllability. Among those innovative candidates, the GAA structure will become the most evolved one due to the ultimate electrostatic controllability because the gate completely surrounds the channel. In this work, a NanoWire is fabricated with aid of a sacrificial SiGe layer embedded bulk substrate. HfO2 is employed as a gate dielectric. The typical electrostatic properties are presented. The capacitor less 1T-DRAM characteristics are attained via the floating body wrapped by GAA as well.

With the advent of 32 nm process technology, the NanoWire FET (fig 1) IV characteristics can be improved in sub nanometer region. The variations in gate length, channel width, gate oxide thickness affects the charge and potential distributions in turn iv characteristics NanoWire FET devices are promising candidates to realize higher speed operation of FET. In NanoWire FET, the channel is surrounded by the gate electrode. This architecture is renowned for good electrostatic control, good sub threshold slope, low leakage current and compatibility with other scaling strategies, such as high k and SOI. However high access resistance, capacitances and self heating effects are challenges for MuGFET (Multiple Gate FET) architectures. The analysis of their behavior is complex because it is influenced by the size, shape, channel orientation and strain induced by the fabrication process. The charge

distributions are to be analyzed with respect to azimuthal co-ordinates threshold voltage in weak inversion region which is affected by the charge distribution. In this paper we present the optimization of the IV characteristics NanoWire FET (fig .2 &3) using the Taguchi method.

CONCLUSION

In this paper nanowire fet iv characteristics were optimized by L8 OA.

ACKNOWLEDGEMENT

We would like to express our sincere thanks to Dr. Prakash R. Apte professor in electrical engineering department, Indian Institute Of Technology ,Bombay,india.

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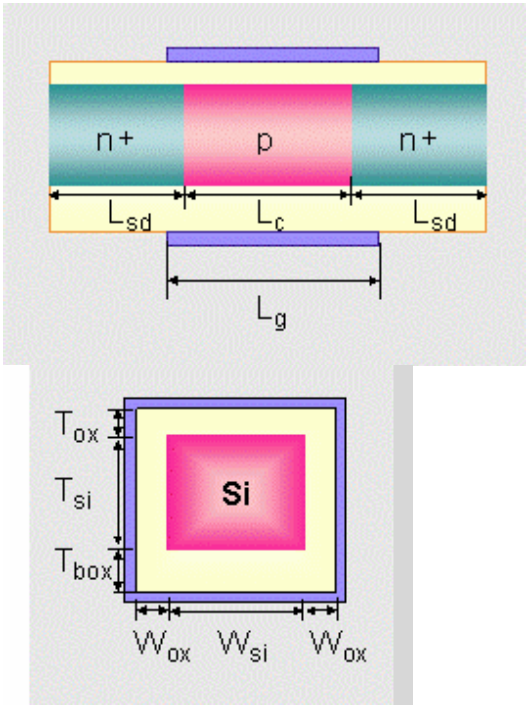

Fig 1. Nanowire fet configuration

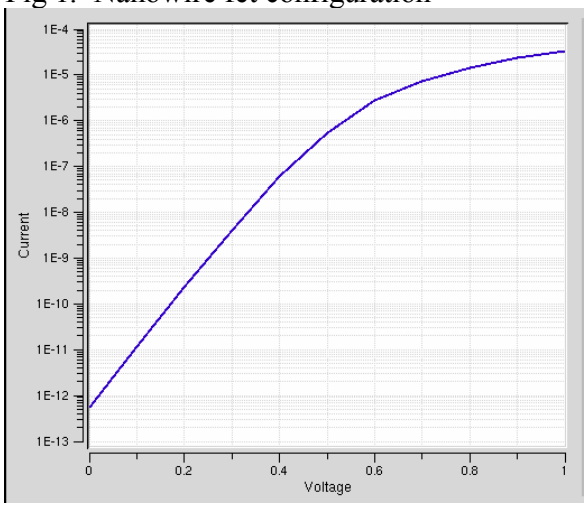

Fig 2 optimized IV characteristics

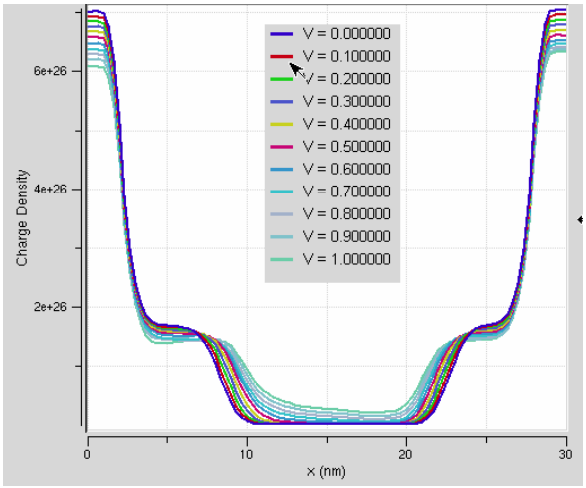

Fig 3 mid cannel chrage density