

TCAD Assessment of Gate-Geometric Multiple Gate Nano-scale $\text{In}_{0.52}\text{Al}_{0.48}\text{As-In}_{0.53}\text{Ga}_{0.47}\text{As}$ HEMT for High Breakdown Voltage

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INTRODUCTION

InP based HEMTs exhibits outstanding RF performances and lower noise figures which find reliable applications in low-noise amplifiers (LNA) designs. However reducing the gate length below 100 nm leads to onset of short channel effects (SCEs) in the devices. Double-gate high electron mobility transistor (DGHEMT) has step-up a new paradigm to reduce short-channel effects (SCEs) in the field of compound semiconductor devices. Increase in gate controllability, double current density and transconductance results in enhanced device performance in terms of SCEs, f_T , f_{max} , and noise parameters over its single gate counterpart [1].

However, with all these advantages DGHEMT still employs InGaAs channel thus making it susceptible to higher impact ionization due to lower InGaAs bandgap resulting in reduced breakdown voltages. Field-Plate (FP) technology (or Gate-Geometries) has been in use to suppress impact ionization, field plate either connected to gate electrodes or biased independently reduces the electric field peak at the gate edge mainly towards the drain side (G-D region) thus improving breakdown characteristics [2].

This field-plate technology becomes more attractive with the scaling of gate-length as the limitation in lithography for submicrometer gate formation involuntarily leads to the formation of various gate geometries like T-Gate, Γ -Gate, Camel-Gate and many more. Therefore, by Field-Plate technology (or Gate-Engineered Technology) the device can be customized as per

the requirements by just modifying the final steps in the fabrication process.

In the present work, Poisson's & Schrödinger equations has been solved with boundary conditions through commercially available Silvaco tool [3] for DGHEMT structure incorporating various gate-geometries. Various physical effects like interface charges, parasitic resistances and capacitances etc have also been taken into account.

CONCLUSION

Analysis shows that T-Gate and Γ -Gate DGHEMT provides good improvement in breakdown voltages while Γ -Gate DGHEMT gives the best trade-off between breakdown and RF performances.

ACKNOWLEDGEMENT

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REFERENCES

- [1] B.G. Vasallo et. al. "Comparison between the Dynamic Performance of Double- and Single-Gate AlInAs/InGaAs HEMTs", IEEE Trans. Electron Devices, vol. 54, pp. 2815-2822, 2007.
- [2] Karmalkar, M. S. Shur, G. Simin, and M. Asif Khan, "Field-Plate Engineering for HFETs", IEEE Trans Electron Devices, vol. 52 pp. 2534-2540, 2005.
- [3] Atlas Device Simulator, Silvaco International., Santa Clara, CA, 2005.

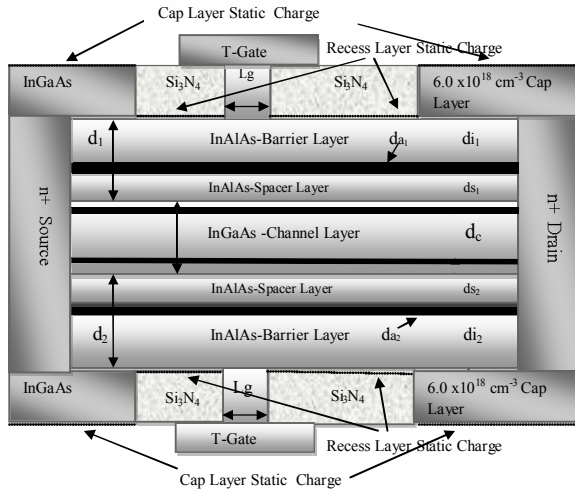


Fig. 1. Schematic of Simulated T-Gate Recessed DGHEMT

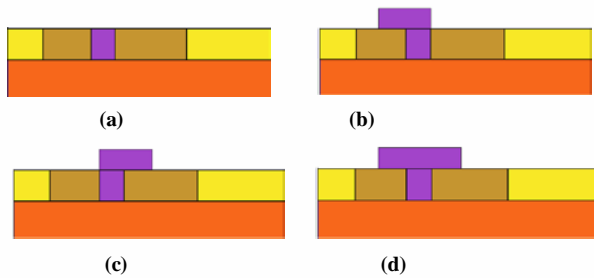


Fig. 2. Cross-sectional view of a) N-Gate (b) IL-Gate (c)Gamma-Gate and (d) T-Gate Geometries.

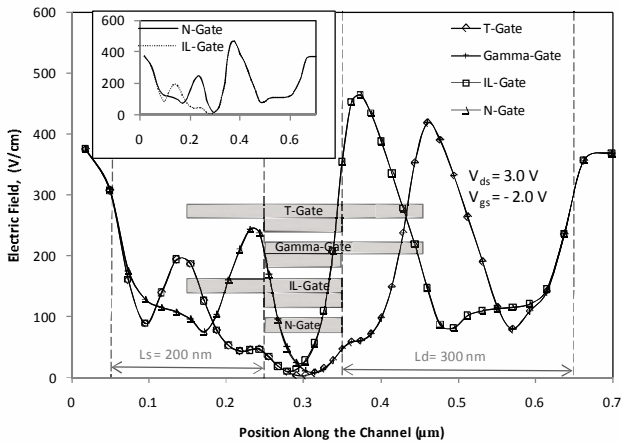


Fig. 3. Electric Field variation along the channel length of different Gate-Geometric DGHEMTs for $L_s=200 \text{ nm}$ and $L_d=300 \text{ nm}$ at $V_{ds} = 3.0 \text{ V}$ and $V_{gs} = -2.0 \text{ V}$.

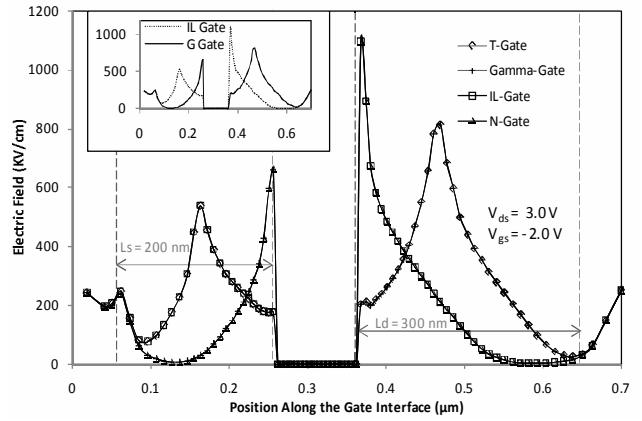


Fig. 4. Electric Field variation along the gate interface of different Gate-Geometric DGHEMTs for $L_s=200 \text{ nm}$ and $L_d=300 \text{ nm}$ at $V_{ds} = 3.0 \text{ V}$ and $V_{gs} = -2.0 \text{ V}$.

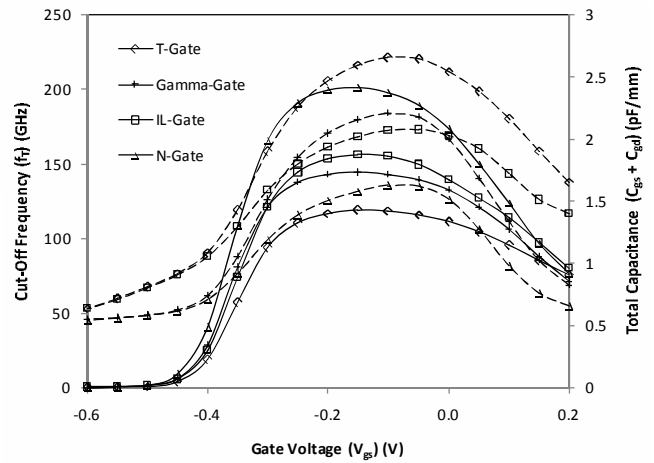


Fig. 5. Cut-off Frequency and Total Capacitance variation with applied gate voltage of different Gate-Geometric DGHEMTs for $L_s=200 \text{ nm}$ and $L_d=300 \text{ nm}$ at $V_{ds} = 1.0 \text{ V}$.