Characterization of the Hot-Carrier Effects in a High-Voltage SOI LDMOS Transistor Based on Full Band Monte Carlo Simulations

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INTRODUCTION

The lateral double-diffused Metal-Oxide-Semiconductor (LDMOS) transistor has attracted tremendous attention due to its high voltage capability and compatibility with complementary metal-oxide-semiconductor (CMOS) process [1]. However, since the electric field in the LDMOS devices is rather high, severe carrier heating occurs [2]. Thus device performance degradation as well as reliability issues caused by the impact ionization generated holes and oxide hot-carrier injection has become a critical problem for the optimal design of LDMOS devices. Conventional drift-diffusion (DD) or hydrodynamic (HD) models lack accuracy in the description of high-energy phenomena, for which Monte Carlo (MC) based simulation has been proved essential [3]. In this paper, we provide characterization of the hot-carrier effects in a realistic HV silicon-on-insulator (SOI) LDMOS transistor based on full-band (FB) MC simulations.

DEVICE AND SIMULATION METHOD

The SOI LDMOS device structure studied in this work as well as its critical dimensions is depicted in Fig. 1, with the device parameters listed in Table I. Colours in Fig. 1 indicate the realistic doping profile of the device. The device has been tuned to achieve a drain BV of 60 V by primary DD simulation in combination with Okuto's avalanche model [4]. Fig. 2 shows the corresponding drain breakdown characteristics of the device.

Starting from the DD results, we then performed simulations on the LDMOS device using our two-dimensional (2-D) FB ensemble MC simulator [5], [6]. The bulk Si full-band structures obtained by local empirical pseudo-potential method are employed [6]. Major scattering mechanisms, including phonon (Ph), surface roughness and ionized impurity scatterings, are considered. Impact ionization (II) is also considered by Thoma's model [7]. Fig. 3 has plotted the phonon scattering and II rates versus energy for different electron and hole bands.

RESULTS AND DISCUSSION

Fig. 4 shows the electric field in the Si film along the dashed line in Fig. 1 under various gate and drain biases. It is observed that two field peaks exist in the drift region, with one lying close to the channel and the other near the drain region. When the device is at on state (V_{gs}=5.0V), the drain peak is commonly much larger than the channel peak, and the change of the drain bias mainly modulates the height of the drain peak. However, as the device switches off (V_{gs} decreases to zero), the channel peak exhibits a big jump over the drain peak. This indicates that the hot-carrier critical spot in the LDMOS device may lie differently depending on the working state of the device. Figs. 5−7 further confirm the above observation by showing the 2-D average electron energy distribution, the energy resolved electron distribution function, and the spatial II rate distribution at V_{gs}=5.0V, V_{ds}=40V and V_{gs}=0, V_{ds}=55V, respectively.

Since II plays an essential role in both the BV and the device performance degradation, we summed up the II generated holes in the whole device and plot the total II hole current in Fig. 8. It is clearly shown that the II hole current increases rapidly with the increase of gate and drain bias.

Fig. 9 shows the energy distribution of the gate average impingement current density induced by carriers in the channel hitting the gate oxide at V_{ds}=40V and different V_{gs}. Electrons dominate the impingement current, and larger V_{gs} corresponds with higher electron hitting energy. Fig. 10 then plotted the total electron current injected into the gate oxide. Larger gate voltage induces larger electron injection current, while the drain bias has rare influence on the oxide injection current.

CONCLUSION

Characterization of the hot-carrier effects in a HV SOI LDMOS transistor based on FB MC simulation is presented. Hot-carrier critical spot dependence on the working state of the device is shown. II induced hole current and oxide injection current related to device degradation are also demonstrated.

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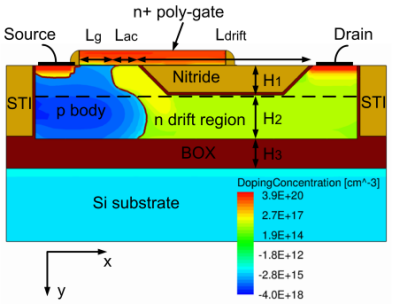

Fig. 1 The SOI LDMOS device structure studied in this work. Colours indicate the realistic doping profile of the device.

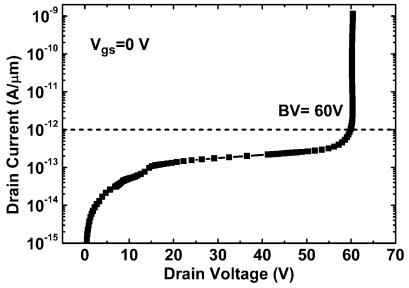

Fig. 2 Drain breakdown characteristics of the LDMOS transistor. The BV is defined as the drain voltage at which the drain current exceeds 1pA/μm at V_{gs}=0 V.

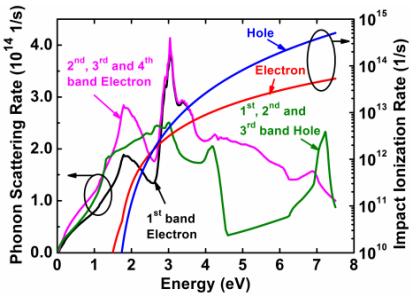

Fig. 3 Phonon scattering and II rates versus energy for different electron and hole bands.

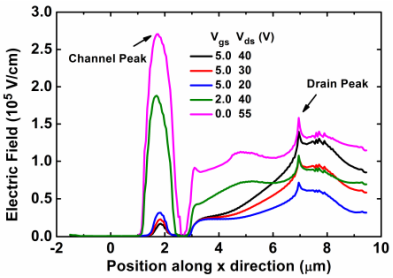

Fig. 4 Electric field in the Si film along the dashed line in Fig. 1 under various gate and drain biases, of which two peaks can be observed.

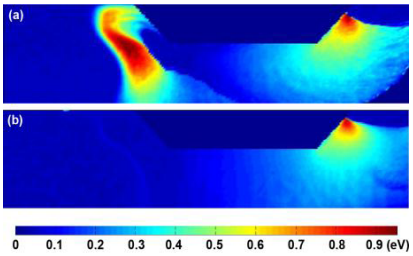

Fig. 5 Average electron energy distribution in the Si film at (a) V_{gs}=0, V_{ds}=55V, and (b) V_{gs}=5.0V, V_{ds}=40V, respectively.

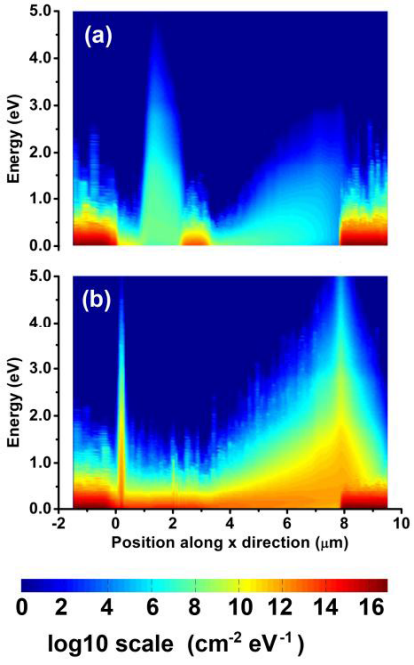

Fig. 6 Energy resolved electron distribution function in the Si film at (a) V_{gs}=0, V_{ds}=55V, and (b) V_{gs}=5.0V, V_{ds}=40V, respectively.

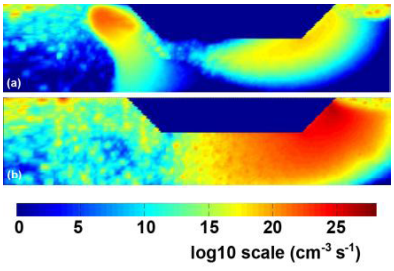

Fig. 7 II rate distribution in the Si film at (a) V_{gs}=0, V_{ds}=55V, and (b) V_{gs}=5.0V, V_{ds}=40V, respectively.

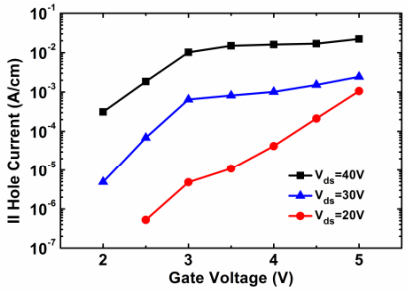

Fig. 8 Total II generated hole current under different bias conditions. The II hole current increases rapidly with the increase of the gate and drain voltage.

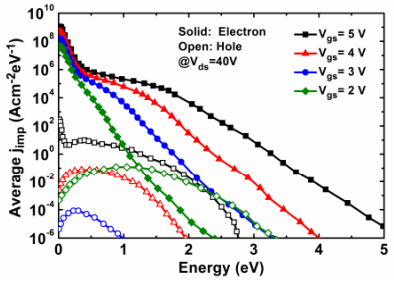

Fig. 9 Energy distribution of the gate average impingement current density induced by carriers in the channel hitting the gate oxide at V_{ds}=40V and different V_{gs}.

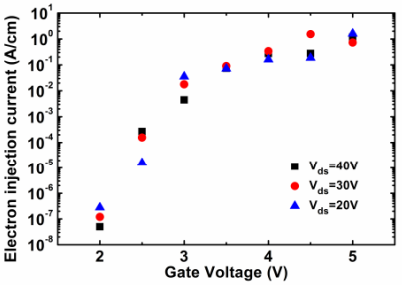

Fig. 10 Total electron injection current into oxide. Larger gate voltage induces larger electron injection current, while the drain bias has rare influence on the oxide injection current.

TABLE I DEVICE PARAMETERS

PARAMETERS	VALUE
Poly-gate length	5 μm
Channel length (L_g)	1 μm
Accumulation region length (L_{ac})	1 μm
Drift region length (L_{drift})	6 μm
Nitride thickness (H_1)	1 μm
Drift region thickness (H_2)	1.5 μm
Buried oxide thickness (H_3)	1 μm
Gate oxide thickness (T_{ox})	20 nm