Self-Heating and Current Degradation in 25 nm FD SOI Devices with (100) and (110) Crystallographic Orientation

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There are two reasons why self-heating in silicon on insulator (SOI) devices is very important: (1) because of the presence of the buried oxide layer (BOX) that is typically made of SiO_2 and has thermal conductivity that is 100 times smaller than the value of bulk Si material (thus representing significant thermal barrier for the heat flow into the substrate); (2) because of the fact that in the active silicon film that has thickness between 10 nm and 70 nm (depending on the technology generation), phonon boundary scattering significantly reduces the thermal conductivity.

To address the problem of lattice heating in nanoscale silicon-on-insulator (SOI) devices in a more rigorous manner from what exists in the literature, we have developed a thermal particle-based device simulator that self-consistently solves the steady-state Boltzmann transport equation (BTE) for the electrons and the energy balance equations for the acoustic and optical phonons [1]. In the past, the thermal simulator has been used in the examination of heating effects in different generations of fully depleted (FD) nanoscale SOI devices. In those analyses we have assumed that the thermal conductivity of the Si layer was temperature independent and characterized by a fixed value of 13 W/m/K that corresponds to a value for 10-nm thick silicon film. In a more recent work, to derive more realistic estimates of the current degradation, we proposed a new theoretical model for the temperature and thickness dependent thermal conductivity based on the work of Sondheimer [2].. Simulation results for different generations of nanoscale FD-SOI devices showed that it is important what model is used in the simulation for the thermal conductivity in properly predicting the average maximum temperature in the hot spot of the device.

In this work, we further extend our investigations on the current degradation in nanoscale FD-SOI devices due to self-heating effects. Here, the focus is on the inclusion of the thermal conductivity tensors as calculated by Aksamija and co-workers [3] using a full-band structure model for the phonon dispersions (see Figure 1). The anisotropy of the effective mass for different crystallographic transport directions has been accounted for using the approach of Rahman and co-workers [4].

In Figures 2 and 3 we present the thermal conductivity profiles in the active Si-layer for 25 nm channel length FD-SOI device for (100) and (110) wafer orientations using our temperature and position dependent thermal conductivity model as compared to the results obtained when using the temperature dependent thermal conductivity tensor model of Aksamija and co-workers [3]. Simulation results show that due to the lower thermal conductivity in the channel region obtained with our model, the lattice temperature in the active Si-layer is higher when compared to the results obtained when using the thermal conductivity tensors model (see Figure 4, right panel). Note, that from thermal point of view, (110) wafer orientation gives better results (lower hot spot temperature). However, from electrical point of view, although the current degradation is lower for (110) orientation, the on-current is smaller compared to the value of the (100)-orientation (see Figure 4, left panel). Thus, one must make a trade-off between the higher temperature in the hot-spot and the higher on-current value.

REFERENCES

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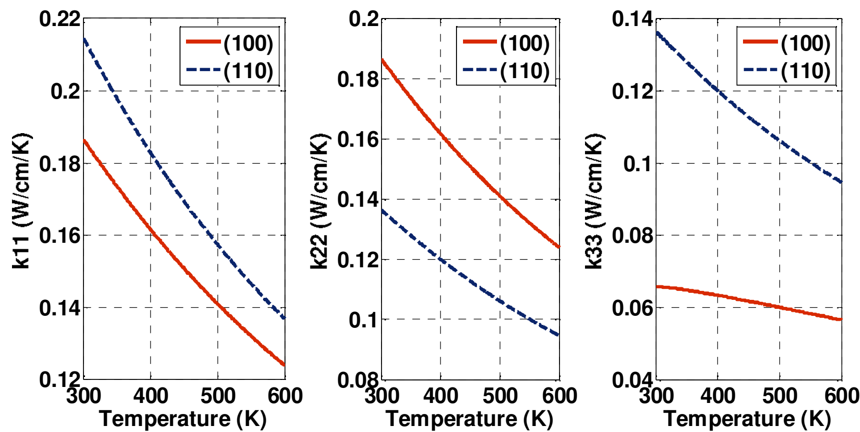


Figure 1. Temperature dependence of diagonal thermal conductivity tensors for (100) and (110) wafer orientations. Off-diagonal elements are very small and can be neglected.

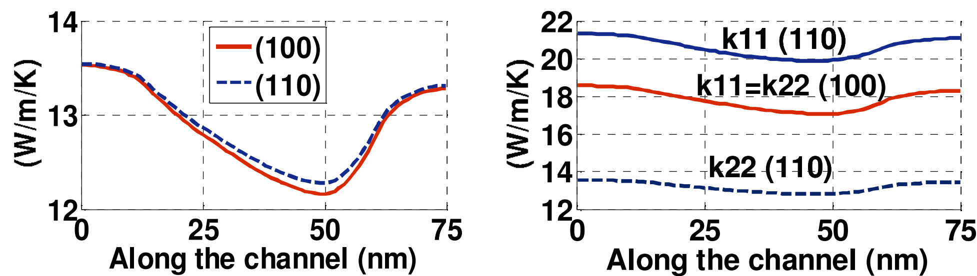


Figure 2. Average thermal conductivity profile in the active Si-layer in 25nm channel length FD-SOI for (100) and (110) wafer orientations using: (left) our thermal conductivity model; (right): thermal conductivity tensors).

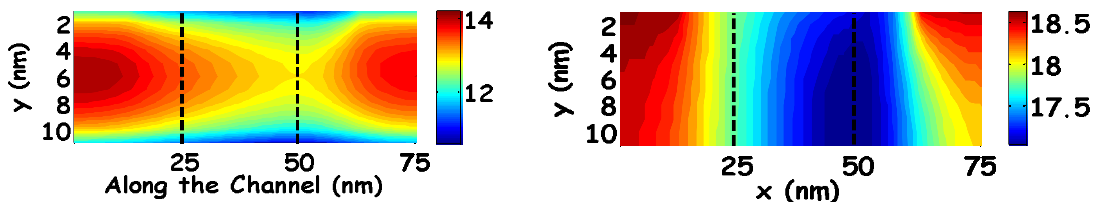
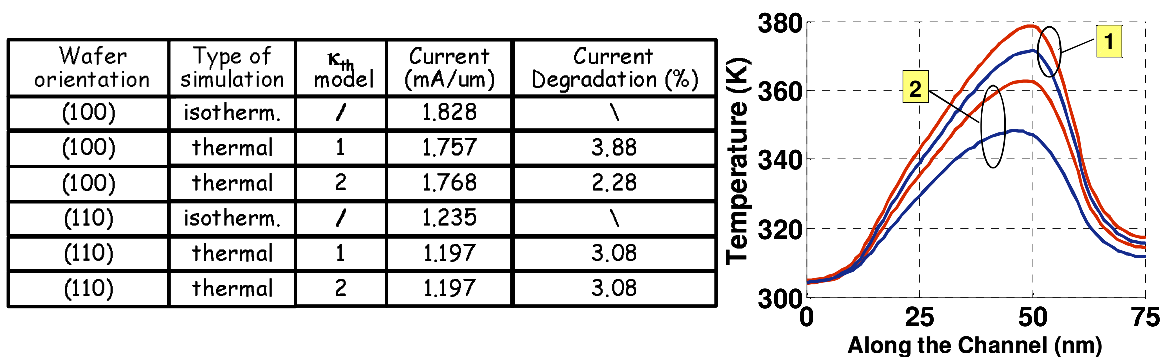


Figure 3. Thermal conductivity profile in the active Si-layer in 25nm channel length FD-SOI for (100) wafer orientation (left: using our thermal conductivity model; right: using thermal conductivity tensors).



Wafer orientation	Type of simulation	κ_{th} model	Current (mA/um)	Current Degradation (%)
(100)	isotherm.	/	1.828	\
(100)	thermal	1	1.757	3.88
(100)	thermal	2	1.768	2.28
(110)	isotherm.	/	1.235	\
(110)	thermal	1	1.197	3.08
(110)	thermal	2	1.197	3.08

Figure 4. Left: Current Degradation for 25 nm FD-SOI and Right: Average Lattice Temperature Profile in the Active Si-Layer. (1-our thermal conductivity model; 2-thermal conductivity tensor); red lines –(100) orientation; blue lines – (110) orientation.