11th International Workshop on Computational Electronics
TU Wien, 25-27 May 2006

Reliability Issues in Power MOSFETs

M. Pölzl, M. Nelhiebel, S. Gamerith, J.Wissenwasser
Infineon Technologies Austria, Siemensstr.2, 9500 Villach, Austria
E-Mail: martin.poelzl@infineon.com

ABSTRACT

Process influences on NBTI as observed on 30nm-GOX trench MOSFETs of two recent power technologies are presented. Both front end of line (FEOL) und backend of line (BEOL) processes are shown to have major effects on the interface quality. A p-channel device serves as demonstrator that nitrogen, introduced into the MOS system during a long-time, high-temperature diffusion step in FEOL processing, plays a major role in the NBTI characteristics. For a n-channel device, we discuss influences of the metallization/passivation BEOL stack on NBTI, but also on initial MOS characteristics and time dependent breakdown. Here, effects are attributed to the release of reactive hydrogen from PECVD deposited silicon-nitride layers.

PROCESS EXPERIMENTS/RESULTS

In case of the p-channel Trench MOSFET a short summary of the different process experiments concentrating on the integration of a long-time, high temperature diffusion step is given in Table 1.

Our observations of parameter degradation of the investigated DMOS devices at NBTI are consistently explained by a diffusion-reaction model ([1], [2]) introduced by Jeppson and Svensson [1] in its basic form. Fig. 1 shows the power-law time dependence of the normalized changes of VT for the different process experiments.

It is found that the degradation is less severe the better the gate oxide was sealed during the body-diffusion step (see fig.1). Actually the fabrication process influences the density of latent defects. As the sealing of the gate oxide during the body drive strongly influences the amount of latent defects we considered the possibility of an atmospheric species intruding into the MOS system during the drive, increasing the latent defect density. The model of varying latent defect density is supported by the long-term drift data in fig.1 as saturation is observed within stress time at different levels.

The device for the BEOL study is a n-channel trench MOS-FET with a 30 nm oxide. Over the trenches a pre-metal dielectric (PMD) is deposited and structured, isolating gate poly from the aluminum source metallization. The metallization stack is completed by inter-level dielectric (ILD) and power metal. For experiments, a PECVD-SNIT (silicon nitride) layer was integrated by different means to the BEOL stack, or the BEOL stack completely omitted (M1 control wafer).

There is a negative correlation between virgin-device interface quality and NBTI characteristics as illustrated in Figs. 2 and 3. The overall GOX-quality defined by TDDB performance is worse when the virgin interface state density is low (Fig. 2). The evolution of Dit upon NBTI stress is displayed in Fig. 3: The ILD/SNIT wafer starts on a very good Dit level, but its Dit rapidly increases and after 15000 s of stress amounts to roughly three times the Dit of the M1 wafer.

DISCUSSION

For FEOL experiments the differences in the absolute values of the degradation are ascribed to different densities of latent defects at the Si-SiO2 interface of virgin devices. A long-time high temperature body diffusion step in nitrogen was detected as the key process concerning NBTI degradation. Based on this observation the role of nitrogen intruding into the system and enhancing the formation of latent defects is discussed.

With the BEOL experiments we demonstrated that deposited silicon nitride layers act as a source of reactive hydrogen [3] with significant influence on the gate oxide of a trench MOS transistor. On the one hand, this reactive hydrogen is more efficient than standard forming-gas tempering and leads to well annealed Si-SiO2 interfaces and good masking of positive bulk-oxide charge. On the other hand the reactive hydrogen has adverse effects on the reliability of the devices, both concerning drift behavior under negative bias temperature stress and

dielectric lifetime measured by TDDB tests. Therefore, backend of line processing must be carefully optimized in order to obtain technologies which show a correct device performance together with the required high reliability.

ACKNOWLEDGEMENTS

We would like to express our sincere thanks to all the contributors to the NBTI investigations (fab, characterisation, technology development and Q department).

REFERENCES

[1] Jeppson K. O.,.Svensson C. M. Negative bias stress of MOS devices at high electric fields and degradation of MNOS devices. J. Applied Physics, vol 48(5) 2004-14 (1977)
[2] Ogawa S., Shiono N.. Generalized diffusion-reaction model for low-field charge-build up Instability at the Si-SiO_2 Interface. Physical Review, vol, 51(7), 4218-30 (1995)
[3] H.K. Sii, J.F. Zhang, R. Degraeve and G.Groeseneken, Relation between hydrogen and the generation of interface state precursors, Microelectron. Eng. 48 (1999) 135

EXPERIMENT	LAYER ON GATE OXIDE DURING BODY DRIVE
body drive before poly deposition	none
body drive before poly deposition + nitride	7 nm CVD-Si_3N_4
standard	p+polysilicon in trench (recessed)
nitride on poly	p+polysilicon in trench + 7 nm CVD-Si_3N_4 (recessed)
body drive after poly deposition	950 nm p+polysilicon

Table 1: overview of FEOL process experiments

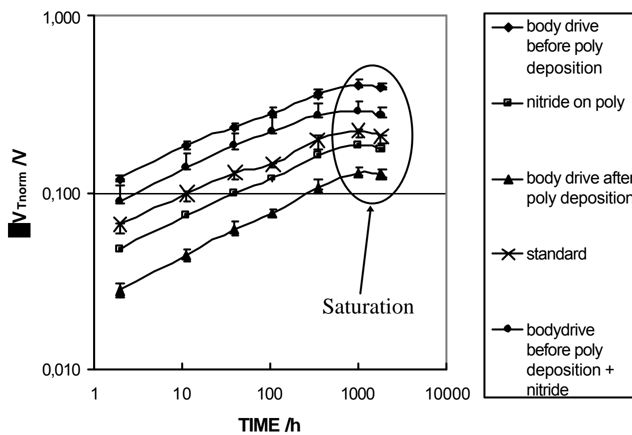

Fig. 1. Time dependence of ΔV_{Tnorm} (shift to more negative values at I_d=1 mA) after 4 MV/cm, 175°C NBTI.

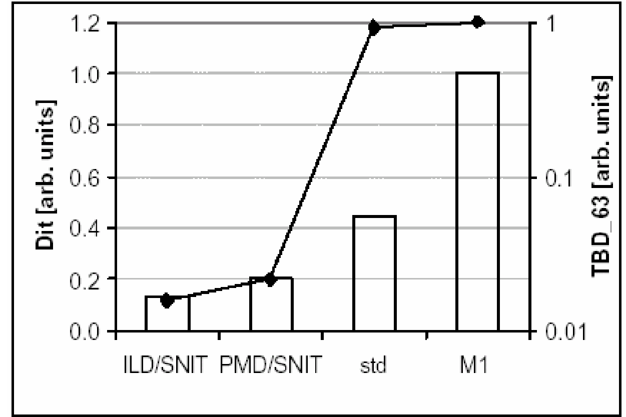

Fig. 2. Dit of virgin device revealed by charge pumping measurements (bars) and characteristic TBD (diamond/line). Roughly, the higher the interface trap density on the virgin device, the better the TDDB performance.

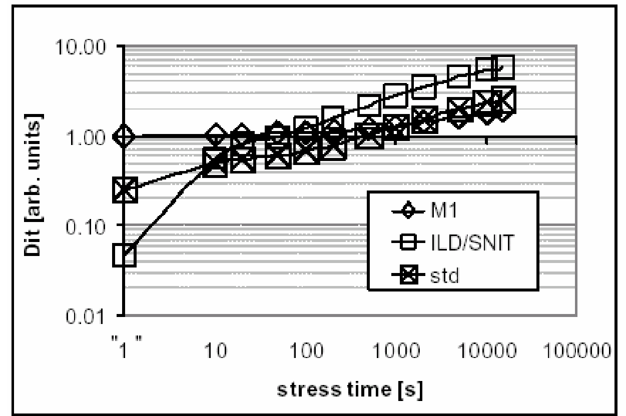

Fig. 3: Evolution of the Dit during NBTI for M1-control (diamonds), ILD/SNIT (squares), and standard process (crossed squares) wafers, respectively. In contrast to the M1 wafer, the SNIT wafer starts from a good level, but traps are rapidly revealed and at the end it is worse than on the M1/std wafers. The values at time “1” are the Dit values of the virgin devices.