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Negative Bias Temperature Instabilities in HfSiO(N)-Based MOSFETs: Electrical Characterization and Modeling

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INTRODUCTION

High-κ gate dielectrics, in combination with metal gates, are extensively studied for the potential replacement of SiON/poly-Si stacks in advanced MOSFETs [1]. One of the most promising high-κ gate oxides is HfSiON [1]. However, reliability issues concerning this material remain a challenge for CMOS devices scaling, in particular NBTI [2]. In this work, the impact of N incorporation in HfSiON layers on NBTI in SiO_x/HfSiON/TaN pMOSFETs is investigated. Like in SiON-based devices, the presence of nitrogen is shown to strongly degrade NBTI immunity of the high-κ gate stack. The enhanced degradation is shown to mainly arise from the generation of slow states in the gate stack. The kinetics, field and temperature dependence of fast and slow states generation are simulated, assuming the former defects to be Si dangling bonds at the Si/SiO_x interface (so-called P_{b0} centers) and the latter to be N-related traps present in the high-κ stack.

EXPERIMENTAL DETAILS

pMOSFETs with 1nm SiO_x/2 nm HfSiO(N) gate stacks and TaN gates were fabricated using a conventional self-aligned flow. The gate stacks received post-deposition anneals in different ambient, i.e N_2, O_2, or NH_3, or exposed to decoupled plasma nitridation (DPN).

RESULTS AND DISCUSSION

The threshold voltage shifts of HfSiO(N)/TaN stacks are presented in Fig. 1 as a function of the electric field across the interfacial oxide, E_{ox} (NBT stress performed at 125 °C). The nitrided stacks present a clear enhanced degradation, compared to the non-nitrided layers. The fraction of (fast) interface states generated during NBTI stress, estimated from charge-pumping measurements at 3 MHz, is presented in Fig. 2 for gate stacks annealed in N_2, NH_3, or exposed to DPN. The enhanced degradation of the nitrided stacks is caused essentially by the generation of slow states, most likely resulting from the trapping of holes (injected from the channel) at N-related defects in the gate stack. The kinetics, electric field and temperature dependence of interface states (N_{it}) generated in a typical HfSiON stack are presented in Fig. 3. These data can be reproduced (Fig. 4) by considering the generation of P_{b0} centers during NBT stress, taking into account the dispersive transport of H^+ away from the Si/SiO_x interface [3]. The kinetics, field and temperature dependence of the slow states (N_{ot}) generated in a nitrided stack are presented in Fig. 5. The N_{ot} generation probability, $P_{gen}=N_{ot}/N_{inj}$, where N_{inj} is the density of holes injected from the channel (assuming slow states are related to the trapping of holes in the gate stack) is shown in Fig 6 as a function of N_{inj}, at different stress voltages. The increase of P_{gen} with $|V_g|$ suggests that these defects are generated during the NBT stress, as opposed to filling of pre-existing traps. Considering the generation of N-related defects in the gate stack (like e.g. N dangling bonds), followed by hole-trapping at these defects, the kinetics and generation of N_{ot} can be well reproduced [4], as shown in Fig. 7 and 8, respectively.

CONCLUSIONS

NBTI degradation of HfSiON stacks was shown to be much enhanced when N was incorporated in these layers. The enhancement was correlated to generation of slow states, most likely related to hole trapping at N-related defects. The kinetics of fast and slow states was successfully simulated, taking into account the generation of P_{b0} defects and N dangling bonds, respectively.

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[2] M. Houssa et al., IEDM Tech. Dig. (2004), p. 121.
[3] M. Houssa et al., Appl. Phys. Lett. **86**, 093506 (2005).
[4] M. Aoulaiche et al., IRPS (IEEE, 2006), p.317.

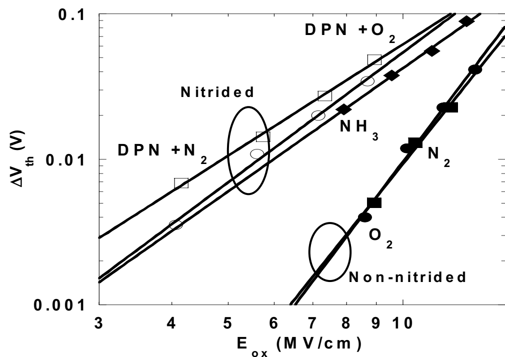

Fig. 1. V_{th} shifts as a function of oxide electric field of HfSiO(N)/TaN gate stacks.

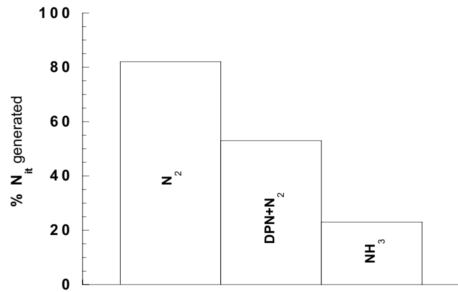

Fig. 2. Fraction of fast interface states, N_{it}, generated during NBT stress of HfSiO(N)-based gate stacks.

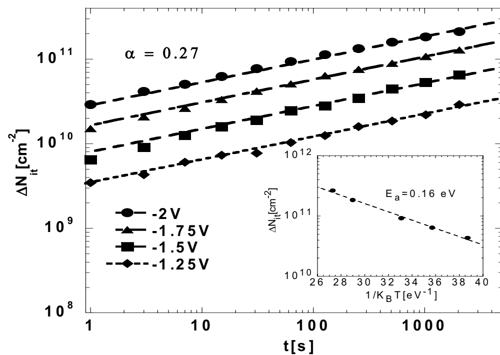

Fig. 3. Kinetics of fast interface states generation of a HfSiON/TaN stack stressed at different V_g. Inset shows N_{it} as a function of inverse temperature.

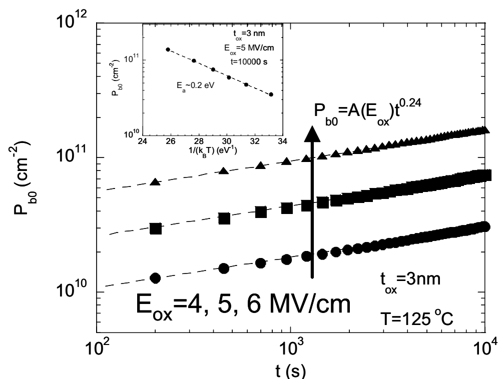

Fig. 4. Simulations of the kinetics and inverse temperature dependence (inset) of P_{b0} center generation within the dispersive H^+ transport model [3].

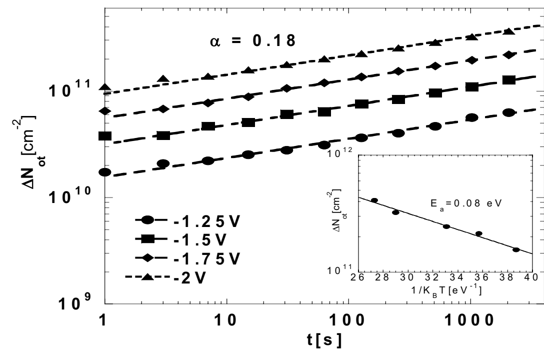

Fig. 5. Kinetics of slow states generation of a HfSiON/TaN stack stressed at different V_g. Inset shows N_{ot} as a function of inverse temperature.

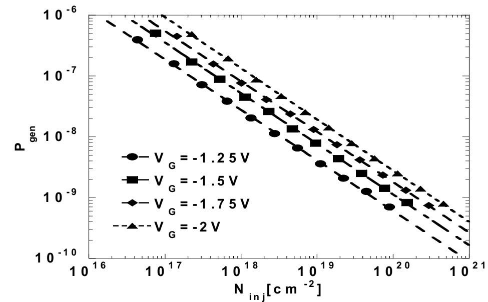

Fig. 6. Generation probability of slow states, as a function of the injected hole density during NBT stress, for different values of V_g stress.

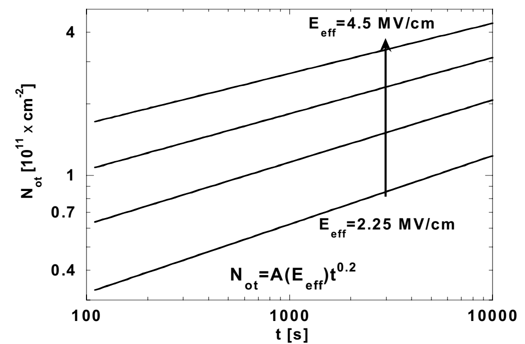

Fig. 7. Simulations of the kinetics of generation of slow states for different values of the electric field across the gate stack.

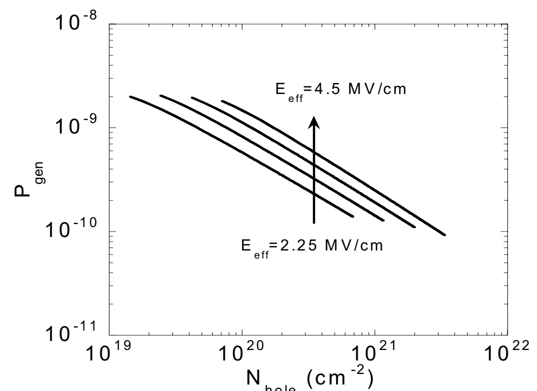

Fig. 8. Simulations of the generation probability of slow states, as a function of the injected hole density, for different values of the electric field across the gate stack.