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On Prospects of Computational Modeling of Reliability Phenomena

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Transistor design has been always been bracketed by the trade-off between performance and reliability. Yet, even a cursory review of the existing mainstream CAD tools shows that optimization of transistor performance (defined in terms of on current, on-off ratio, power dissipation, circuit delay, etc.) has been the primary focus on the CAD tools and reliability considerations have only been used to define a static guard-band (typically plus-minus 15%) for IC design. Although there have been a number of attempts to develop reliability simulators, these stand-alone reliability tools have never been integrated within the mainstream CAD software.

In recent years, however, the scenario is beginning to change. As scaling becomes difficult and design margin for high-performance IC becomes small, a static, worst-case guard-band limited design is both wasteful and unsustainable. Indeed, CAD tools that allow IC-specific optimization for both reliability and performance would allow additional design margin for a given technology node. In this presentation, I will review the development both TCAD models to predict performance degradation for specific operating conditions as well as IC-design approaches to optimize overall design in response to specific degradation. Below, we briefly discuss the status of modeling approaches to various degradation mechanisms.

Negative Bias Temperature Instability (NBTI) has been known to be an important degradation mechanism for PMOS transistors since 1970s. Jeppson et al. analyzed the NBTI phenomena within a Reaction-Diffusion (R-D) model and was able to explain the observed time-dependence ($t^{0.25}$) during the stress phase as well as relaxation behavior when the stress is removed. In this version of R-D theory, the negative gate bias on PMOS transistors allows a hole-assisted dissociation of Si-H bonds at the Si/SiO_2 interface. Atomic H diffuses away from the interface, leaving behind a depassivated, dangling Si bond that acts as interface trap. Recent refinement of the original R-D model have been able to interpret long term saturation characteristics, the relevance of measurement delay, frequency independence of AC lifetime, etc. The key feature of this refined R-D model is the realization that atomic H diffusion must be complemented by diffusion of molecular H_2 to interpret NBTI experiments consistently. The R-D model equations are now well defined and can be included in TCAD software. Finally, the R-D model is phenomenological and therefore the model parameters (e.g., forward and reverse dissociation rates, diffusion coefficients, etc.) must be extracted from experiments and/or first-principle theory. There have been considerable progress on both fronts in recent years.

There have also been some progress in translating the TCAD NBTI models to appropriate VLSI design algorithms such that the circuits can be optimized for a given power-delay product. Both logic as well as memory circuits have been considered. The Lagrangian-based transistor sizing, activity rebalancing, redundancy algorithms, etc. show considerable promise, although it is still too early to predict if the algorithms would be practical for large designs.

Time-Dependent Dielectric Breakdown is another important reliability consideration for modern IC design and has been particularly important since late 1990s as oxide thickness has scaled to sub

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5nm regime. It is widely believed that under typical operating conditions, the dielectric breakdown is soft and the breakdowns only contribute to the total leakage current. This increase in gate leakage is a predictable function of operating conditions, oxide thickness, and area of the oxide and its implication on transistor performance can easily be analyzed with TCAD and SPICE models both for logic as well memory circuits. Many companies use in-house simulators to predict these performance characteristics, although there have been no academic or commercial software available for general use.

Although *Hot-Carrier Degradation* is no longer the dominant degradation mechanism for core technology it once was in late 1980s and early 1990s, the continued scaling of channel length makes HCI a relevant design consideration. In addition, HCI degradation remains an important design consideration for Flash memories as well high-voltage devices like LDMOS and DeMOS. The early models of HCI discussed the relative merits of hot electron and/or hot hole degradation and the research results were encapsulated in compact models suitable for TCAD analysis. The relatively compact form of the models helped define the SPICE model and have been used in HCI circuit simulator like BERT, RELY, and more recently GLACIER.

Radiation Induced Single Event Upset (SEU), *Radiation Induced Gate Leakage* (RILC), and *Radiation Induced Gate Rupture* are important design considerations for modern ICs and there have been consideration progress in modeling these radiation induced phenomena. For example, the accurate modeling of ion tracks have been demonstrated, the modeling of SEU with 3D device simulators now provides predictable estimates, and the RILC and radiation induced gate breakdown has been considered within the same framework as TDDB. In addition, the circuit implication of correlated multi-bit failure as well as development of appropriate error correction codes are active research areas, results from which can be translated to CAD models.

In short, the physics of many important reliability phenomena are now generally well understood and therefore a systematic effort may allow development of a new generation of TCAD and CAD tools that can simultaneously optimize for performance and reliability of integrated circuits.

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