Electronic and Transport Properties of Silicon Nanowires

F.Sacconi[1], M. Persson[1], M. Povolotskyi[1], L. Latessa[1], A.Pecchia[1], A. Gagliardi[2], B. Aradi[2], T. Frauenheim[2,3], A. Di Carlo[1,*]
[1]Dept. Electronics Eng. , Univ. of Rome "Tor Vergata", via Politecnico 1, 00133 Roma, Italy
[2]University of Paderborn, Warburger Str. 100, 33100 Paderborn, Germany
[3]on move to Center for Computational Material Science, University of Bremen, Germany, 28359 Bremen.
[*]e-mail: aldo.dicarlo@uniroma2.it

INTRODUCTION

The current process of scaling of semiconductor devices to the nanoscale size can lead to great improvements in the device performance, such as increased speed and low-voltage operation.
In Si metal-oxide-semicoductor field effect transistors (MOSFETs), the scaling of channel length requires that gate performs an effective control action. This can be achieved with new technology solutions such as silicon nanowires, which allows 3D control of the channel. Silicon nanowire structures can be obtained by using both a "top-down" approach, mainly based on etching techniques and a "bottom-up" approach, where silicon nanowires are directly synthesized. Both approaches are well suited for the realization of nanoMOSFET, however, structural and electronic properties of top-down and bottom-up nanowire are different. During nanowire synthesis atomic position are relaxed while in the top-down process the silicon nanowire maintains a typical bulk atomic structure.

This work present a detail investigation of structural, electronic and transport properties of silicon nanowires and silicon nanowire based nanoMOSFET

METHODS AND RESULTS

Electronic properties of etched silicon nanowires are investigated with two different approaches, namely the Empirical Tight-Binding (ETB) model and the Linear Combination of Bulk Bands (LCBB) method. Within the ETB the system is described by using a nearest-neighbour $sp^3d^5s^*$ parameterization for silicon. We consider both hydrogenated and SiO_2 terminated silicon surface. SiO_2 is wrapped around the Silicon cell, by means of an interface which avoids dangling bonds and surface states; we use the β-crystobalite polytype of SiO_2 which is described with a second-nearest-neighbour sp^3 parameterization [1]. With this model, we have calculated electronic energies, dispersion, minimal gap and effective masses of silicon nanowires structures (see Figs.1-3). LCBB approach is based on an empirical pseudopotential description of the Si structure[2]. Single-particle eigenstates of electron and holes are obtained as a linear combination of conduction or valence bands states of bulk silicon. Here SiO_2 is modelled as a potential barrier. Dispersion relation for two typical silicon nanowires as obtained with LCBB is shown in Fig. 4. A comparison between LCBB and ETB will be given.

The structure of synthesized Si nanowires (freestanding and functionalized) is obtained by minimizing the total energy by using an approximated DFT tight-binding method (DFTB). Figure 5 shows a calculation of the final geometry of a (110) oriented hydrogenated silicon nanowire.

Transport properties of nanowires are obtained by applying the Green function method to both empirical and DFT tight-binding description.[3] Figure 5 shows the calculated IV characteristics for the relaxed silicon nanowire. The non-equilibrium Green function (NEGF) approach has been considered to describe nanoMOSFET devices based on Silicon nanowires. Figure 6 shows the calculated potential profile and charge density for a silicon nanowire based nanoMOSFET.

REFERENCES

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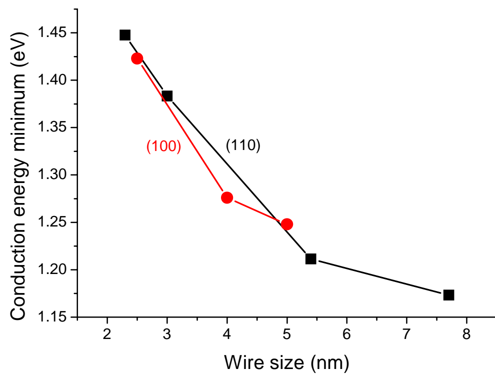

Fig. 1 Conduction band minimum as a function of silicon nanowire size for both (100) and (110) oriented nanowires. ETB results

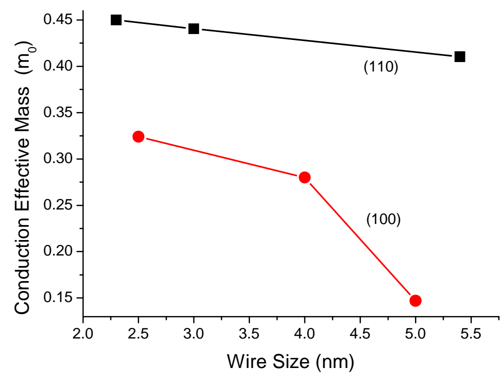

Fig. 2 Effective mass as a function of silicon nanowire size as obtained with ETB.

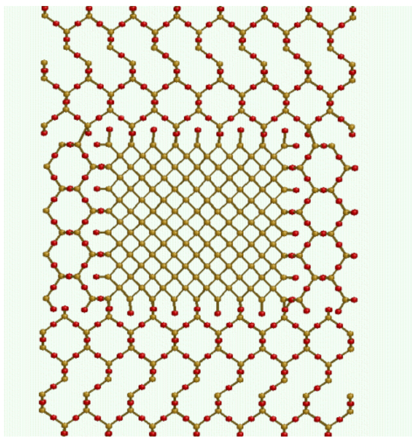

Fig. 3 Structure of the silicon nanowire surrounded by SiO_2

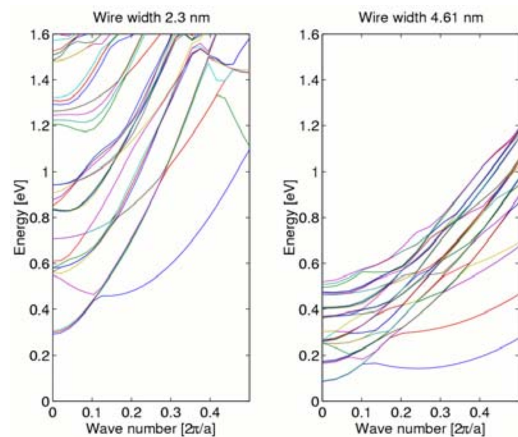

Fig. 4 band dispersion of two Silicon nanowires as obtained with LCBB.

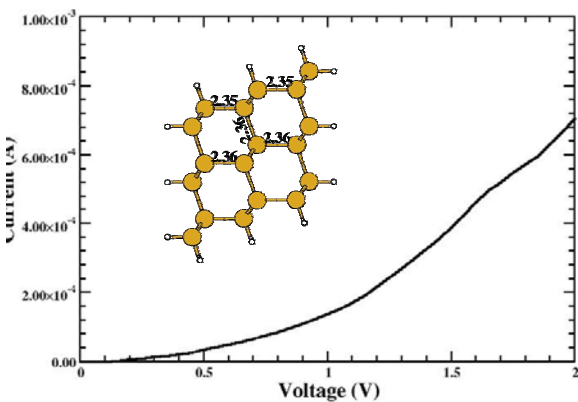

Fig. 5 Current flowing in a Silicon nanowire as a function of applied voltage (inset) Relaxed structure of the hydrogenated silicon nanowire.

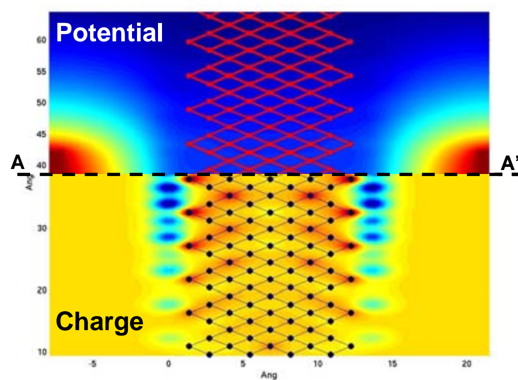

Fig. 6 NEGF results of a coaxially gated silicon nanowire. The system is symmetric with respect to AA' line. Gate bias is 0.5 V. Charge is referred as a difference with respect to zero bias condition.