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Phonon Exacerbated Quantum Interference Effects in III-V Nanowire Transistors

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Abstract

In recent years, a great deal of attention has been focused on the development of quantum wire transistors [1,2] as a means of extending Moore's Law. Here we present, results of fully three-dimensional, self-consistent quantum mechanical device simulations of InAs tri-gate quantum wire transistors. The effects of inelastic scattering have been included as real-space self-energy terms [3]. We find that the position of dopant atoms in these devices can lead to significant departures in performance when inelastic processes are considered.

Device Structure

In Fig. 1, we show a schematic of the device geometry under consideration. Here the exact device dimensions (multiples of the lattice constant) have been included in this simulation to aid in the inclusion of the discrete dopants. In each device that we consider, the channel length is 9.69 nm , the thickness of the InAs layer is 9.09 nm, and the channel width is 8.5 nm. The source and drain of the device are *n*-type with a doping density of 6×10^{18} cm^{-3}, while the channel of the device is considered to be *p*-type, but undoped. The gate material is assumed to be platinum and the gate oxide on each side is composed of 1 nm of hafnium oxide (HfO_2). Underneath the device, we have assumed a generic insulating substrate.

Results and Discussion

In Fig. 2, we plot the I_d-V_g characteristics for an InAs quantum wire transistor both in the case of only impurity scattering and with the effects of polar optical phonons, intervalley ($\Gamma \rightarrow X$ and $\Gamma \rightarrow L$) phonons and acoustic deformation potential scattering. Here, we see that the current is not too terribly degraded from the elastic case to including inelastic processes. Speaking strictly from a device standpoint, the devices with inelastic process included tended to have better subthreshold swing and I_{on}/I_{off} ratios than did the devices with elastic processes. This is due to the fact that the scattering in the source is relatively weak thereby producing reductions I_{off} but not significantly limiting I_{on}.

In Fig. 3, we plot where several dopants in the source of the device lie in the middle of the semiconductor close to the channel entrance. As a result, the carriers entering the channel of the device have their incident energy significantly altered. The carriers now see a significant increase in the amount of scattering they undergo before entering the channel causing a major reduction in current.

In Fig. 4(a) and (b) we plot the electron density in the middle of the device for the elastic and inelastic cases respectively. Clearly as a result of the increased scattering, the electrons begin to pile up in the source around the potential spikes near the channel entrance in the inelastic case. Furthermore, we also see a reduced electron density in the channel and the drain of the device as a result of the backscattering near the channel entrance.

We confirm this assertion in Fig. 5, where we plot the difference in potential between the elastic and inelastic cases of this device. We find that charge density increases of ~0.38 k_bT in the source of the device and decreases of 0.38 k_bT in the channel and drain corresponding to increases or decreases in charge density of one-half order of magnitude.

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References

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[2] M.J. Gilbert and D.K. Ferry, J. Appl. Phys, Accepted for publication.
[3] M.J. Gilbert, R. Akis, and D.K. Ferry, J. Appl. Phys. **98**, 094303 (2005).

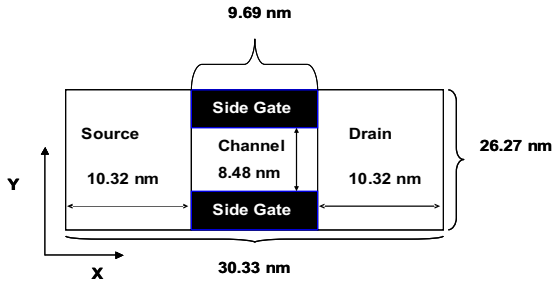

Fig. 1. Schematic of the device geometry in the *x*-*y* plane

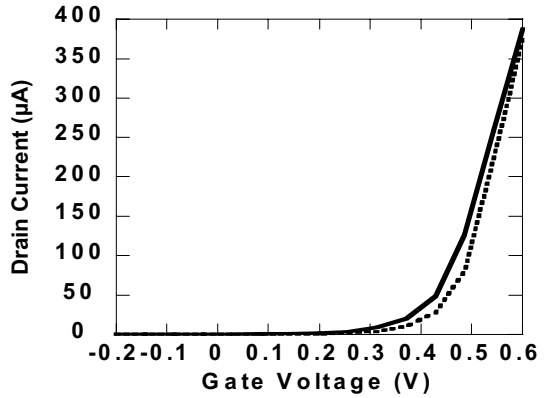

Fig. 2. Id-Vg curves for an InAs tri-gate quantum wire transistor with elastic (solid) and inelastic (dotted) scattering included.

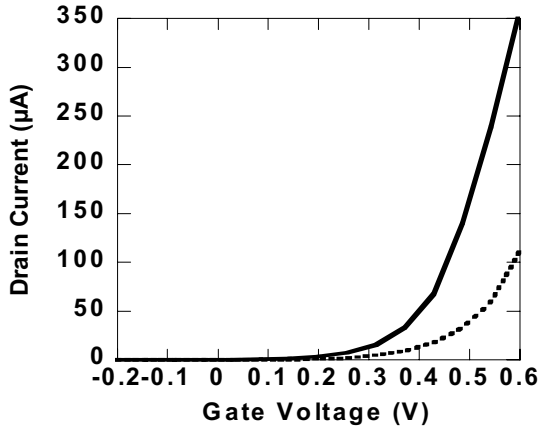

Fig. 3. Sample Id-Vg curves for an InAs tri-gate quantum wire transistor with elastic (solid) and inelastic (dotted) scattering included. Here the dopants reside close to the channel entrance.

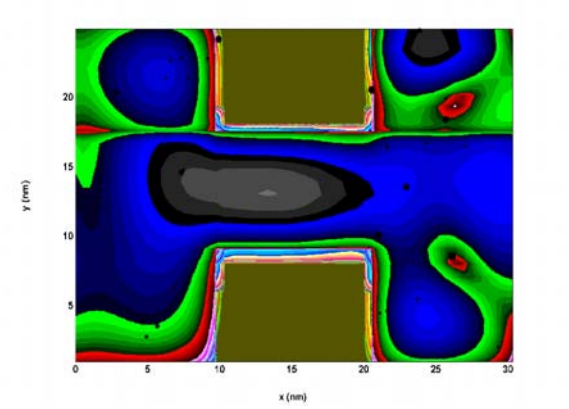

Fig. 4(a). Electron density at Vg = 0.6 V and Vd = 0.6 V taken at a depth of 7 nm into the device with only elastic processes included.

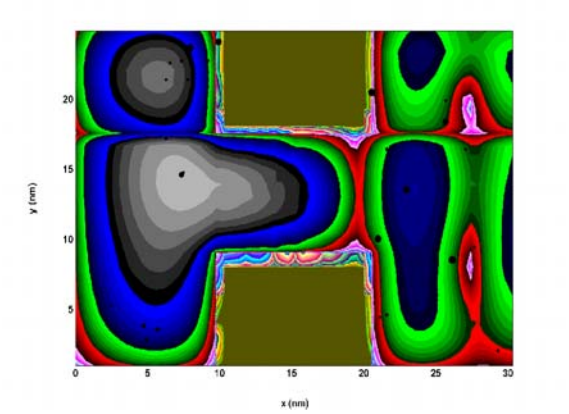

Fig. 5. Electron density at Vg = 0.6 V and Vd = 0.6 V taken at a depth of 7 nm into the device with elastic and inelastic processes included.

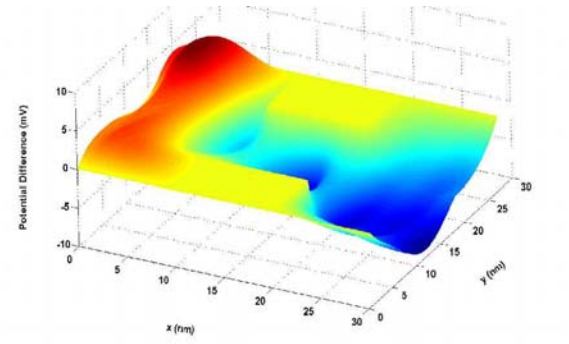

Fig. 6. Potential change at Vg = 0.6 V and Vd = 0.6 V taken at a depth of 7 nm between only elastic and combined processes.