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Effect of Elastic Processes and Ballistic Recovery in Silicon Nanowire Transistors

D. Basu, M. J. Gilbert, and S. K. Banerjee
Microelectronic Research Center, University of Texas at Austin, Austin, TX 78758 USA.
e-mail: mgilbert@mer.utexas.edu

INTRODUCTION

Scaling of silicon devices is approaching a limit where a single gate may fail to retain effective control over the channel region. Silicon nanowire transistors (SNWT) show great promise, in terms of scalability, performance, and ease of fabrication. Here we present results of self-consistent, fully 3D quantum mechanical simulations of SNWTs using recursive scattering matrices [1]. We find that the addition of surface roughness (SR), in conjunction with the presence of impurity scattering, causes additional quantum interference which forces the SNWT operational parameters to increase their variation. However, we find that the quantum interference and elastic processes can be overcome to obtain nearly ballistic behavior in devices with preferential dopant configurations.

DEVICE SIMULATION

In Fig. 1, we show a schematic of the device geometry we consider. The *p*-type channel is undoped. Its dimensions are 9.8 nm in length, and 8.1 nm in width. The source and drain regions, 18.47 nm wide, 10.47 nm long. The silicon film thickness is a uniform 6.51 nm high. The source and drain regions are *n*-type and doped 10^{20} cm^{-3}. Fig. 2 shows a typical interface for the devices studied. SR scattering is included by using a non-uniform mesh, with mesh spacing down to 0.36 nm at the interface. In this study, we model the Si-SiO_2 interface roughness using an exponential auto-correlation function, with r.m.s. roughness 0.3 nm and correlation length 1.3 nm which is consistent with experimental values [2].

RESULTS AND DISCUSSION

Fig. 3 shows I_D-V_G results for the quantum wire transistor for four different SR patterns, keeping the same dopant distribution. The SR causes a reduction of I_D while threshold voltage (V_T) increases. We also find that the subthreshold slope (SS) remains nearly constant, while the I_{on}/I_{off} ratio increases. This is due to the fact that SR scattering is more effective for carriers in the low field regime. These findings are summarized in Tab. 1. At high V_G, higher I_D in rough devices indicates that SR causes interference with the carriers in the channel. This not only shifts the longitudinal states in the channel, but, under constructive situations, can increase I_D.

Fig. 4. shows I_D-V_G results for the SNWT for four random dopant distributions, neglecting SR. Wide variations in I_D result from different location of the dopants. Stronger reflections are caused by shallow dopants located near the source-channel interface. Such a device turns on later than others (circles in Fig.4). On the other hand, a device that has few dopants close to the source-channel interface shows nearly ballistic behaviour (square markers). In the remaining devices, there are dopants close to the source-channel interface, but buried deeper in the device, causing I_D-V_G characteristics to lie between the extremes.

In Fig. 5, we show the same set of devices with a fixed SR included. The increased spread in the SNWT parameters due to SR is evident from Tab. 1. The deviation of I_D from that of the smooth device is particularly large for one particular device (○ markers in Fig. 5), where the shallow dopant ions are also happen to be in close proximity to a rough section of the top gate-oxide-channel interface. The carriers scattered from the interface get trapped in the potential field of the dopants. As gate bias increases, I_D approaches the smooth device values since the carrier energies is now enough to overcome the quantum interference.

REFERENCES

[1] M. J. Gilbert and D. K. Ferry, J. App. Phys. **95**, 7954 (2004).

[2] S. M. Goodnick, D. K. Ferry, et. al., Phys. Rev. B **32,** 8171 (1985).

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Parameters	V_T	ΔV_T	SS	ΔSS	I_{on}/I_{off}	$\Delta I_{on}/I_{off}$
Units	(mV)		(mV/decade)			
No SR. Fixed dop. dist.	99	—	67.71	—	897	—
Diff. SR. Fixed dop. dist.	144.9	2.5	68.79	0.39	1119	43.66
No SR. Diff. dop dist.	95.1	8.4	68.66	1.98	735.96	72.15
Fixed SR. Diff. dop dist.	127.5	19.1	70.33	2.43	741.38	145.24

Table 1. Mean parameter values for various simulations.

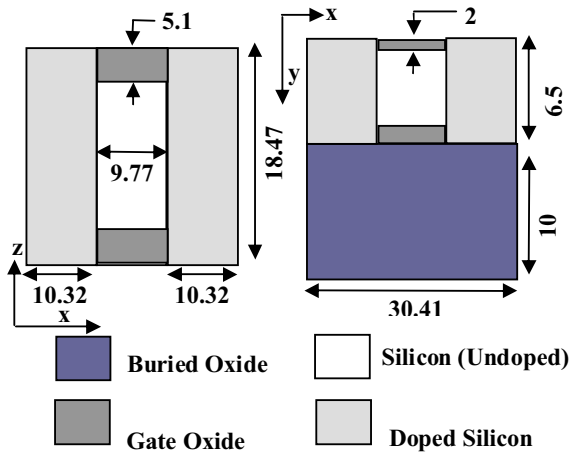

Fig. 1. Schematic of the simulated device, showing – in left, the device from top, and in right, a vertical cross-section through the middle of the device. All dimensions are in nm.

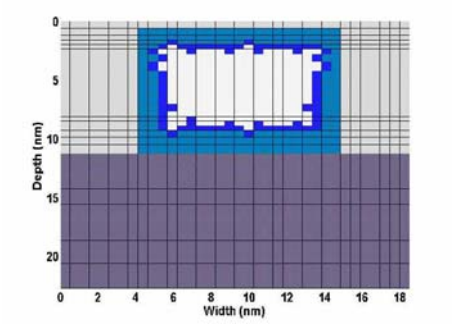

Fig. 2. A typical cross-section of the simulated nanowire, showing irregularities at the Si-SiO_2 interface due to SR.

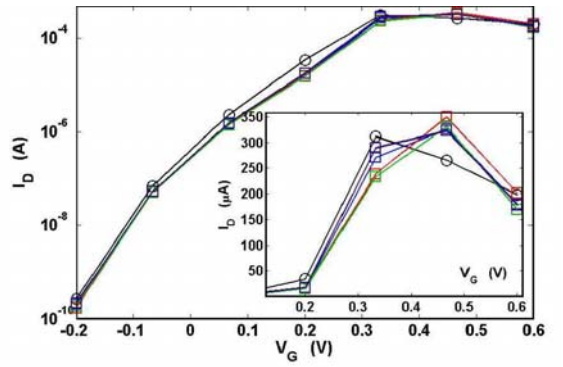

Fig. 3. I_D -V_G for four different SR patterns, keeping the dopant distribution same at V_D = 0.6 V. Square markers (□) denote I_D including SR, circles (○) imply without SR. Inset: linear scale.

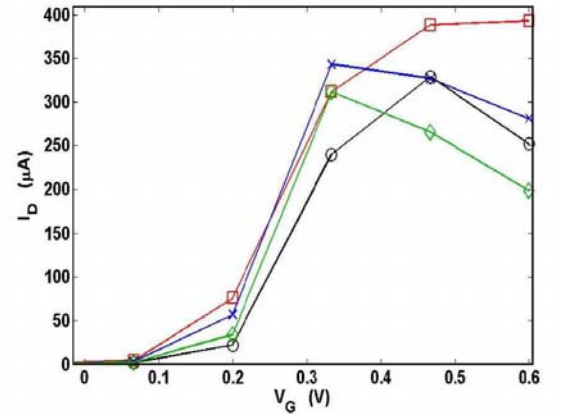

Fig. 4. I_D – V_G for four different random dopant distributions, without roughness at the Si-SiO_2 interface at V_D = 0.6 V.

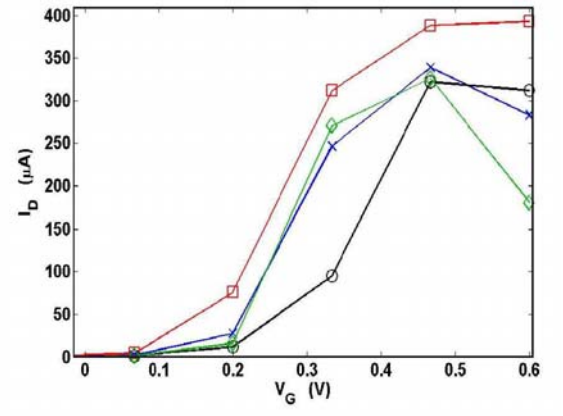

Fig. 5. I_D –V_G for same four discrete dopant distributions of Fig. 4. SR is considered and an identical pattern is used for all the simulations. The drain voltage is held constant at 0.6 V.