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Study of the Cutoff Frequency of Optimized SOI MESFETs

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The Schottky Junction Transistor (SJT) [1] is a novel device suitable for micropower circuits applications due to its high mobility values with respect to its conventional counterpart - the silicon MOSFET. Since the mobility of the SJT or SOI MESFET is higher than that of SOI MOSFET in subthreshold and the on state regime, obviously the cutoff frequency should be higher as well for SJT [2]. Even though the SJT device offers higher f_T, there is no garuntee that the same device will also offer optimum performance in terms of the voltage gain.

To calculate the cutoff frequency and to determine optmized device dimensions, we have developed a transport model, based on the solution of the Boltzmann Transport Equation, for modeling *n*-channel silicon-on-insulator (SOI) MESFETs using the Ensemble Monte Carlo technique. All relevant scattering mechanisms for the silicon material system have been included in the model [3]. Major modifications in the existing device simulator have been made in the description of the carrier flow from the gate contact to the conduction channel (as shown in Fig. 1) which takes place mainly by tunneling through the Schottky barrier at the silicon/$CoSi_2$ interface. The tunneling probability is calculated using the transfer matrix approach for piece-wise linear ptentials[4]. To optimize the perfomence of the device structure in terms of figures of merit, like cutoff frequency and voltage gain, different devices have been simulated for different doping densities, varous SOI layer thickness and with different gate lengths. Then, a mathematical model is employed to identify which device shows optimum performance.

A prototypical transfer character for a device with gate length L_g =50nm is shown in Fig. 2 and is used in calculating the cut off frequency f_T. More precisely, the cut-off frequency f_T is extracted by using $f_T=g_m/2\pi C_g$, where g_m is the transconductance and C_g is the gate capacitance of the device under consideration. A sample extracted value for the cut-off frequency is 83.6GHz, as shown in Fig. 3 for a device with L_g=50nm and t_{si} = 25nm, which is quite high with respect to the cutoff frequency of an equivalent MOSFET device. These data are also compared with projected experimental values derived from experimental results of 0.6μm gate length SJT that are shown in Fig. 3. Similarly, the voltage gain is found from the transconductance and the output conductance for the same device dimension which is shown in Fig. 5. Then, the mathematical model is employed where the product of the cutoff frequency and voltage gain is determined for a particular device dimension and the device which has maximum product is chosen to be the optimum one.

From this simple model it is found that the device with a gate length 90nm, silicon film thickness of 20nm and doping density in the channel of 5×10^{17} cm^{-3} is the optimum one (see Fig. 6) and exhibits 33.3GHz cutoff frequency and 25.3 voltage gain. Due to this enhanced cutoff frequency and voltage gain, we can conclude that the SOI MESFET device is a suitable candidate for application in r.f. micropower circuit design for both digital and analog applications.

REFERENCES

[1] T. J. Thornton "*Physics and Applications of the Schottky Junction Transistor*", *IEEE Trans. Electron Devices,* 48, 2421 (2002).

[2] K. Tarik, S. Ahmed, D. Vasileska, T. Thornton, "*Subthreshold mobility modeling of SOI MESFETs*", Journal of Computational Electronics, Volume 3, Numbers 3-4 Pages: 243 - 246 2005.

[3] M. V. Fischetti et al., "*Long-Range Coulomb Interactions in Small Silicon Devices. Part I: Performance and Reliability*" J. Appl. Phys., 89, 1205(2001).

[4] B. Winstead and U. Ravaioli, *Simulation of Schottky barrier MOSFETs with coupled quantum injection/ Monte Carlo technique*", IEEE TED 47, 1241 (2000).

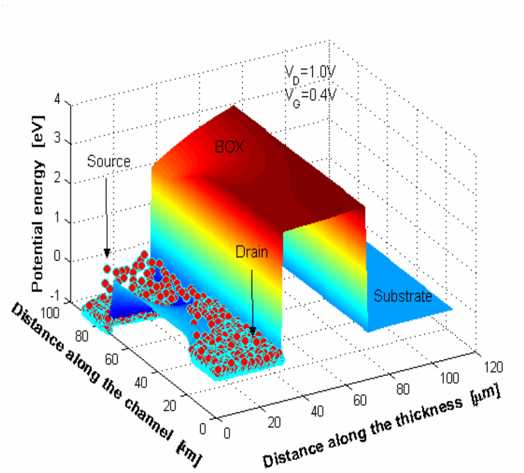

Fig. 1. Two dimensional potential profiles where electrons are flowing interacting with the top interface of the BOX layer and few of them are tunneling through the schottky barrier.

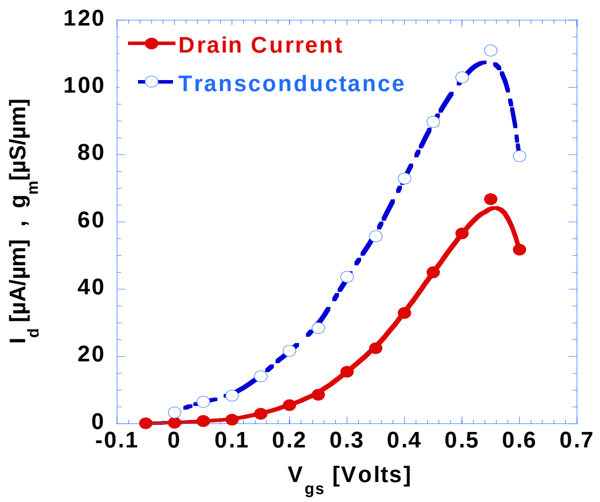

Fig. 2. Transfer characteristics and variation of transconductance with gate voltage at $V_d = 0.1$V.

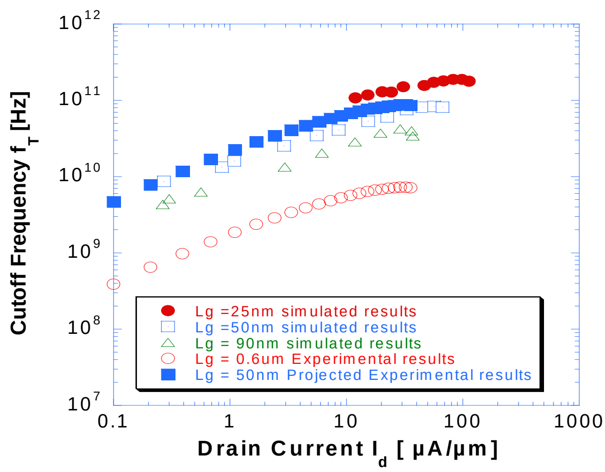

Fig. 3. Simulated and experimentally obtained cutoff frequency

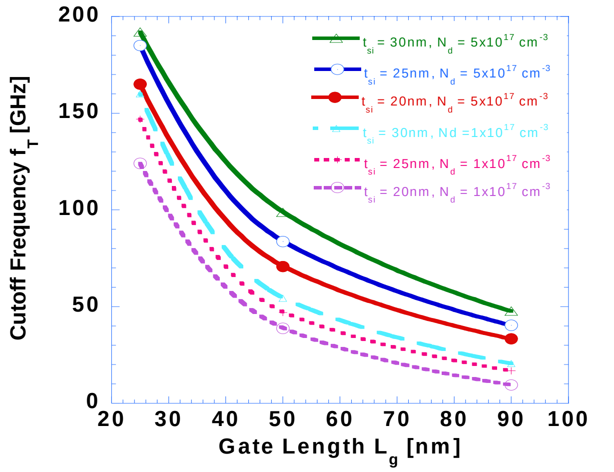

Fig. 4. Variations of cutoff frequency for different device dimensions to find the optimized dimension.

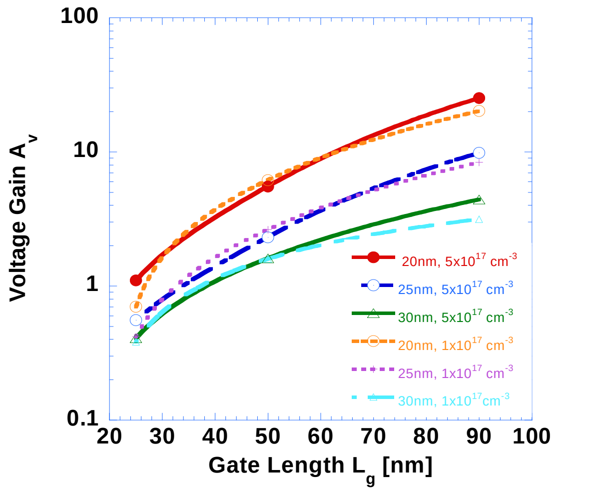

Fig. 5. Variations of voltage gain for different device dimensions to find the optimized dimension.

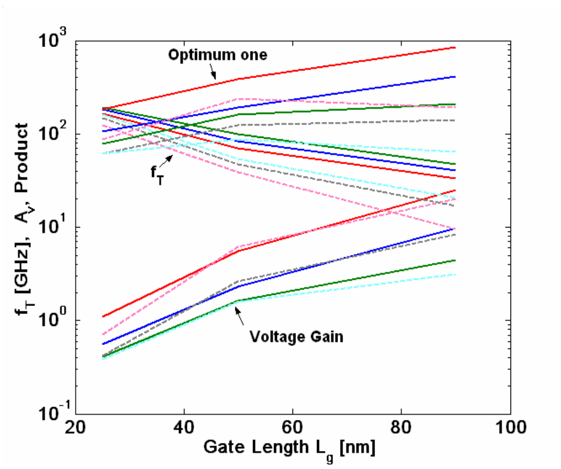

Fig. 6. Determination of the optimized device dimension.