Analysis of Nano-Scale MOSFET Including Uniaxial and Biaxial Strain

Ryo Tanabe, Takahiro Yamasaki, Yoshio Ashizawa, and Hideki Oka
Fujitsu Laboratories Ltd., 50 Fuchigami, Akiruno, Tokyo, 197-0833, Japan
e-mail: tanabe.ryou@jp.fujitsu.com

INTRODUCTION

The mobility improvement technology using strained channel is being actively researched for further scaling. Mainly, two methods have being discussed. One method is that we use biaxial strained Si which is formed on the SiGe buffer layer. The other method is that we use uniaxial strained Si. For example, SiN Cap film, SiGe-SD and SiC-SD. In addition, several surface orientations and channel directions have been considered to use best performance in strained Si.

In this paper, we focus uniaxial and biaxial strain technologies, and an optimum combination of strain method and channel direction is studied.

UNIAXIAL STRAIN CHARACTERISTICS

First of all, uniaxial strain characteristics are studied. The states of the strained Si band are calculated by using the first principles pseudo-potential band calculation program PHASE [1]. The transport analysis was discussed by Fujitsu Full Band Monte Carlo Simulator FALCON.

In Fig.1, calculated double gate (DG) structure is shown. Fig.2 shows the results of uniaxial characteristics. We calculated the state of strain from -2.0%(compressive) to +2.0%(tensile). We considered two channel directions, <100> and <110>. As shown in Fig.2, for NMOS, I_{on} increases by tensile strain and decreases by compressive strain respectively. It is the almost same tendency for both directions, but <100> direction has larger merit than <110>. On the other hand, for PMOS, the dependency for strain is small for <100>. <110> direction has large dependency for strain. Current increases by compressive strain largely.

Next, we will discuss the difference of <100> and <110> for NMOS. In Fig. 3 and 4, we show the valley energy and population for both directions. Although for <110> uniaxial, all Δ4fold valleys are isotropic, Δ4fold valleys show anisotropic property for <100> uniaxial strain. As pointed out in [2], additional electron population leads smaller conductivity mass.

BIAXIAL STRAIN CHARACTERISTICS

Next, we will show the results of biaxial strain. In Fig.5, the I_{on} improvement ratios are shown as a function of strain. In biaxial strain condition, for NMOS, I_{on} increases by tensile strain, and decreases by compressive strain respectively. For PMOS, I_{on} increases by both tensile and compressive strain. Fig.6 shows the dependencies of current direction. 0 deg is <110> direction and 45 deg is <100> direction. For electron, current improvement ratio is almost the same for any angle in unstrained state, but electron has anisotropic property in strained state. <100> direction has maximum merit of strain. For hole, <100> direction has maximum merit for both unstrained and strained states. Finally we will show the relationship between scaling and ballistic rate in Fig.7 and 8. I_{on} improvement ratio decreases as gate length scaled down. But, the merit of strain will be kept to 5nm gate length especially for <100> direction. Ballistic ratio in <100> direction is also higher than that of <110> direction. This is because of effective mass differences between <100> and <110> direction.

DISCUSSION

In Table 1, each I_{on} improvement ratio is summarized for both uniaxial and biaxial (L_g=30nm). The combination of biaxial tensile strain and <100> current for NMOS, and compressive uniaxial strain and <110> channel for PMOS are optimum methods for current enhancement. However, for technological difficulties and process cost, the way that we use uniaxial tensile strain and <100> channel direction for NMOS and uniaxial compressive strain and <110> channel direction for PMOS is one of candidate method.

CONCLUSION

We focused both uniaxial and biaxial strain technologies, and an optimum combination of strain method and channel direction was studied. The way that we use biaxial tensile strain and <100> channel direction for NMOS and uniaxial compressive strain and <110> channel direction for PMOS is considered to be the most realizable combination.

REFERENCES

[1] http://www.fsis.iis.u-tokyo.ac.jp/theme/nanoscal/software/
[2] H. Irie et al., IEDM Tech. Dig., pp.225 (2004).

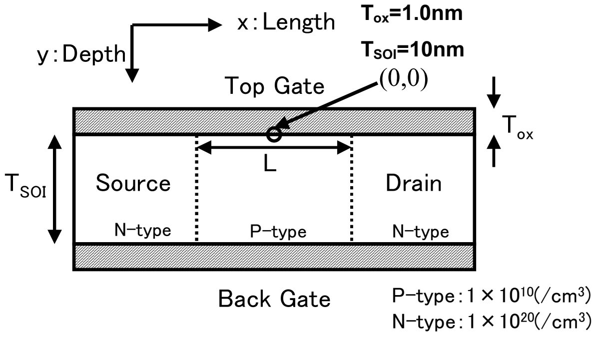

Fig. 1. Calculated DG structure

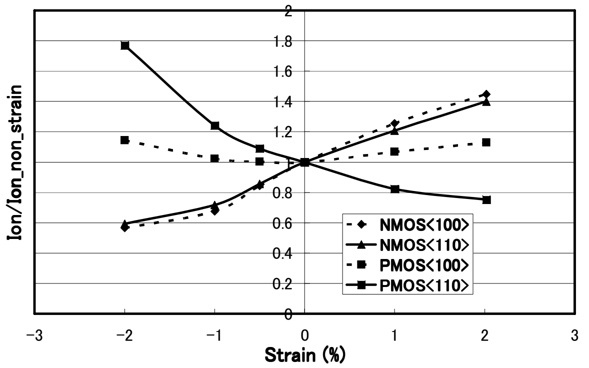

Fig. 2. Uniaxial strain characteristics for both <100> and <110> direction

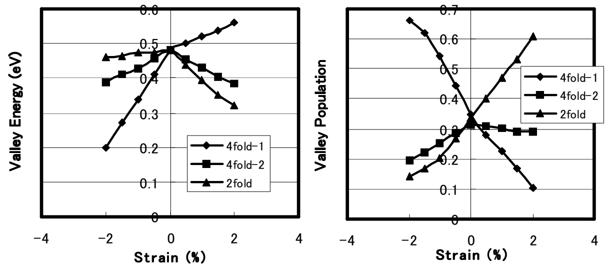

Fig. 3. Valley energy and valley population for <100> uniaxial strain

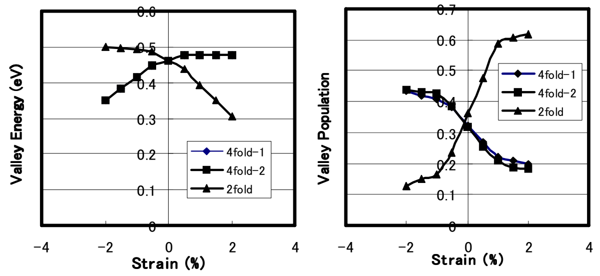

Fig. 4. Valley energy and valley population for <110> uniaxial strain

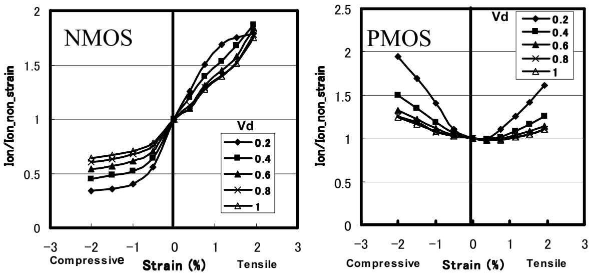

Fig. 5. Biaxial strain characteristics for <110> direction

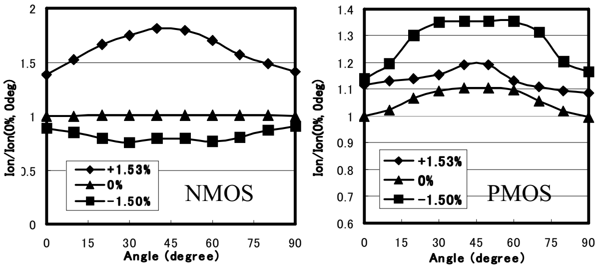

Fig. 6. The dependencies of current direction

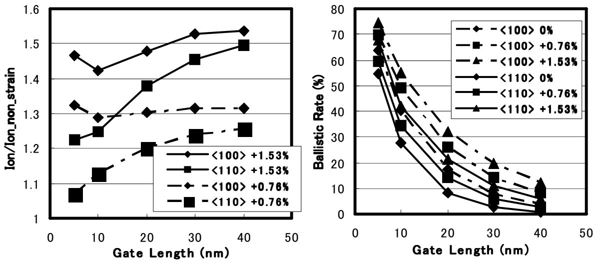

Fig. 7. I_{on} improvement and ballistic rate with scaling (NMOS)

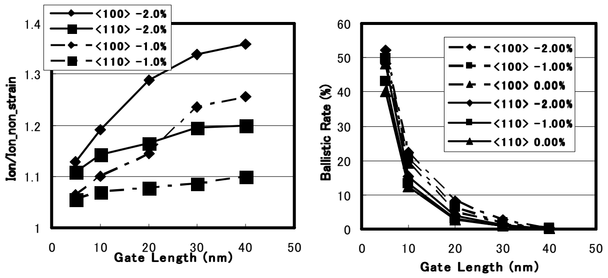

Fig. 8. I_{on} improvement and ballistic rate with scaling (PMOS)

Table 1. Summary of I_{on} improvement ratios for several strain and current conditions (L_g=30nm)

	Channel	NMOS	PMOS
Uniaxial	<100>	1.47(tens.)	1.16(comp.)
	<110>	1.38(tens.)	1.80(comp.)
Biaxial	<100>	1.72(tens.)	1.34(comp.)
	<110>	1.65(tens.)	1.20(comp.)