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Electrothermal Monte Carlo Simulation of Submicron Wurtzite GaN/AlGaN HEMTs

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The miniaturisation of device features has been accompanied by an exponential increase of the heat generated within the devices. As a result, the development of electrothermal models is necessary to study the effect of self-heating on the performance of submicron devices. This paper presents results from the application of an electrothermal Monte Carlo (MC) simulator to submicron wurtzite GaN/$Al_{0.15}Ga_{0.85}N$ High Electron Mobility Transistors (HEMTs). The simulator iteratively couples a MC electronic trajectory simulation with a fast Fourier series solution of the Heat Diffusion Equation (HDE). The simulator models the effect of acoustic and optical phonons mediating intravalley electronic transitions, and phonons mediating intervalley electronic transitions. Ionised impurities, alloy disorder, electron-electron and impact ionisation scatterings, and the effect of electron degeneracy are also included in the simulations. The simulator uses a simple five-valley spherical non-parabolic model of the bandstructures of GaN and AlGaN, as this work focuses on the coupling of electronic and thermal transport. The simulations are performed self-consistently, by solving Poisson's equation in two dimensions every 1.0 fs. Polarisation induced charge at the GaN/AlGaN interface is modelled as a sheet of ionised donors placed at the interface. Polarisation effects also induce a net negative charge at the top surface of the AlGaN layer, a feature which is included in the simulations. The simulator extracts the power density distribution within the simulated region (see Fig. 1) using the net phonon emission approach [1]. The generated distribution is fed to the HDE solver to determine the temperature distribution. The HDE is solved in two dimensions using an analytical thermal resistance matrix technique [2], which solves for the temperature over the simulated region while considering the conditions at the boundaries of the semiconductor die (see Fig. 2). The subsequent MC iteration is performed with the updated temperature distribution characterising the lattice temperature in the simulated region.

Preliminary results are shown in Fig. 3, which are obtained using a SiC substrate. The electrothermal device I_{ds}-V_{ds} characteristics, shown in Fig. 3(a), demonstrate the thermal droop effect, which is known to be caused by device self-heating. Fig. 3(b) illustrates how the temperature distribution is non-uniform with a peak value occurring at the top of the device between the drain end of the gate and the start of the drain region. Fig. 3(c) demonstrates how the value of the peak temperature depends on the applied bias. The substrate material type plays an important role in the device thermal management, and thus the effect of using different substrate materials is investigated. More results have been generated using Si, GaN and single crystal sapphire substrates. Under the same biasing conditions, the use of a SiC substrate is shown to provide the lowest peak temperature and the lowest current reduction (upon the inclusion thermal self-consistency). The use of a sapphire substrate gives the worst thermal performance, as it is a poor thermal conductor. A reduction in the device die length is observed to raise the peak temperature in the simulated region and increase the extent of the thermal droop. The effect of introducing a negative polarisation charge of different concentrations at the top surface of the device is also examined. The presence of the surface charge modifies the electric potential distribution in the simulated region, and thus affects the values of the source-drain current and the peak temperature.

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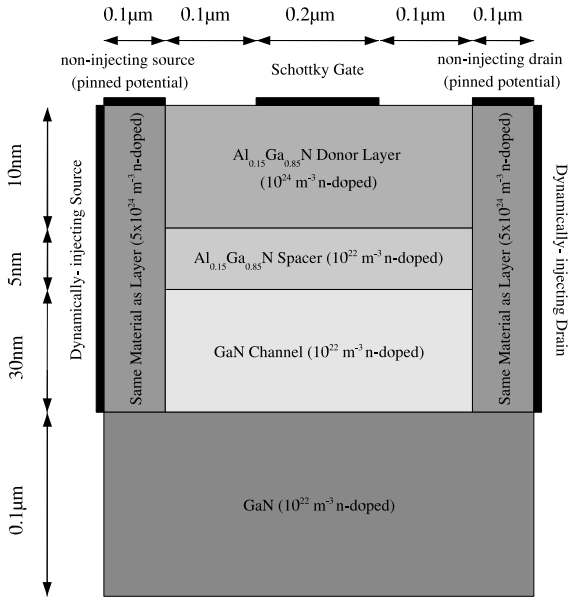

Fig. 1. The electronically simulated region of the GaN/AlGaN HEMT.

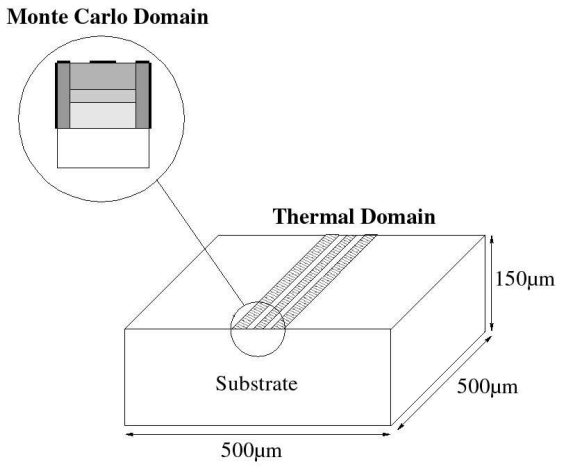

Fig. 2. The electronic MC and the thermal simulation domains.

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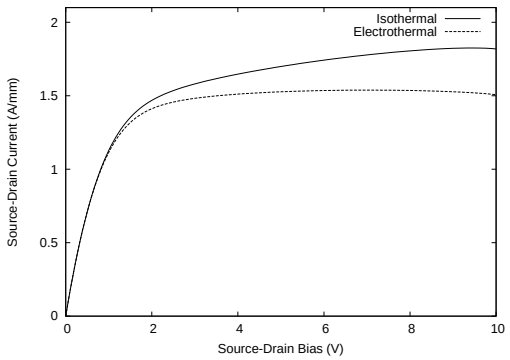
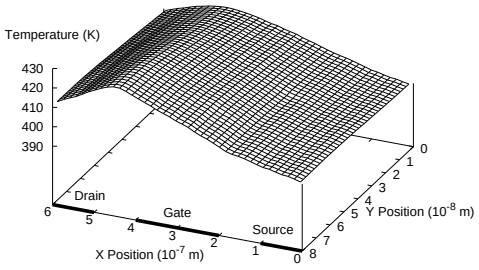
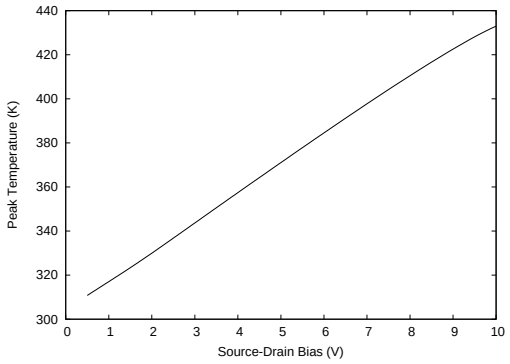


(a)



(b)



(c)

Fig. 3. (a) I_{ds}-V_{ds} characteristics of the HEMT at a source-gate bias of 1.0 V; isothermal simulations are performed at 300 K. (b) Temperature distribution at a source-gate bias of 1.0 V and a source-drain bias of 10.0 V; $x = 0$ is the start of the source region, $x = 6 \times 10^{-7}$m is the end of the drain region, $y = 8 \times 10^{-8}$m is the device top surface. (c) Variation of the peak temperature with the source-drain bias at a source-gate bias of 1.0 V.