11th International Workshop on Computational Electronics
TU Wien, 25-27 May 2006

On the Impact of High-κ Gate Stacks on Mobility: A Monte Carlo Study Including Coupled SO Phonon-Plasmon Scattering

G. Ferrari*, J.R. Watling*, S. Roy*, J.R. Barker*, P. Zeitoff†, G. Bersuker†, and A. Asenov*
*Device Modelling Group, Dept. Electronics & Electrical Engineering, University of Glasgow
G12 8LT Glasgow, United Kingdom. E-mail: G.Ferrari@elec.gla.ac.uk
†SEMATECH, 2706 Montopolis Drive, Austin, Texas 78741, USA.

The scaling of MOSFET architecture, as dictated by the International Technology Road Map for Semiconductors, is reaching its limit. A major problem is the requirement for extremely thin gate oxides and high channel doping, the consequence being low device performance and high-gate leakage. The fulfilment of the next generation technology requires changes in terms of both new materials and architectures.

HfO_2 based high-κ oxide materials have been identified as the most promising candidates to replace SiO_2 as insulators. A thickness of about $t_{ox} \approx 0.7nm$ is required for SiO_2 gate oxides to obtain the required gate capacitance. The introduction of high-κ dielectrics allow a physically thicker oxide, while maintaining the gate capacitance, to reduce the gate leakage current.

Our Monte Carlo (MC) simulator includes all the relevant scattering mechanisms necessary for the accurate modelling of electron transport in Silicon. In Fig.1 we show the results for the universal mobility curve in the case of SiO_2 as insulator.

It is well known [1, 2] that high-κ materials lead to a mobility degradation due to the coupling of carriers in the channel to surface soft-optical (SO) phonons in the vicinity of the dielectric interface. These SO modes are induced by the longitudinal-optical (LO) phonons in the insulator. The coupling of LO phonons through long range polarisation fields to the free-carrier system gives rise to collective plasma modes and electron excitations. These hybrid modes (polarons) are affected by Landau damping [1].

We have introduced the new scattering mechanisms relevant for high-κ dielectrics in our MC simulator. Landau damping is taken into account and plays an effective role at high momentum transfer, as shown in Fig.2. A comparison has been performed between the mobility of SiO_2 and HfO_2. We have obtained the universal mobility curve for HfO_2 and the results are presented in Fig.3: the severe degradation in mobility is evident.

The gate-stack system is further complicated by the presence of an interfacial layer at the interface between the channel and the insulator. The effect of this layer is twofold: on the one hand it will effectively mitigate the strong interaction with the SO phonon modes of the high-κ dielectric, resulting in a higher mobility; on the other hand the introduction of a layer with a lower-κ value lowers the total effective capacitance of the gate oxide. We have simulated a system with an interfacial layer of pure SiO_2, obtaining the results presented in Fig.4. In Fig.5 we present a surface plot of our results for the mobility as a function of both the interfacial layer thickness and of the perpendicular field applied. The mobility increases when the SiO_2 layer becomes thicker, having as a limit the mobility of SiO_2; moreover the agreement with the experimental data [3] is qualitatively and quantitatively excellent. The slight discrepancy that we observe at low interfacial layer thicknesses may result from the interfacial layer composition, being SiO_x in nature rather than the SiO_2 at these thicknesses.

The composition of the interfacial layer is still to be understood. It may be an SiO_2 layer with oxygen deficiency, resulting in an SiO_x layer, or an SiO_2 layer enriched by Hf [4], thus to be an $Si_{1-x}Hf_xO_2$ layer. We have performed simulations for the first case based on the experimental values of κ of the interfacial layer [3]. To understand the second case, we have simulated the universal mobility with an alloy of $Si_{1-x}Hf_xO_2$ as dielectric, and the results are presented in Fig.6.

REFERENCES

[1] M.V. Fischetti, S.E. Laux, J. Appl. Phys. **89**, 1205 (2001).
[2] J.R. Watling, L. Yang, A. Asenov, J.R. Barker, S. Roy, IEEE Trans. Dev.& Mats Rel. **5**, 103 (2005).
[3] G. Bersuker, private communication (2005).
[4] M.H. Evans, M. Caussanel, R.D. Schrimpf, S.T. Pantelides, IEDM Tech. Dig., 611 (2005).
[5] S. Takagi, A. Toriumi, M. Iwase, H. Tango, IEEE Trans. on Elec. Dev. **41**, 2357 (1994).

ISBN 3-901578-16-1

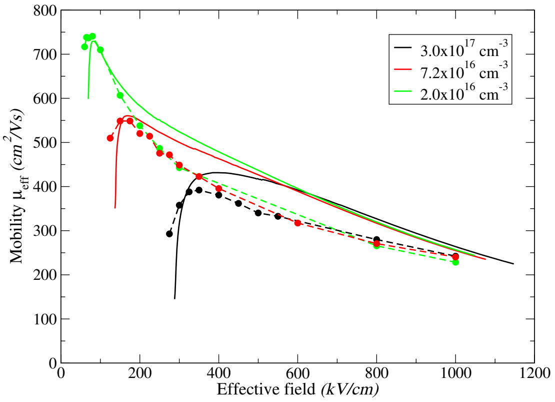

Fig. 1. Electron mobility in the inversion layer at 300 K versus effective field E_{eff}. The results are shown for three values of substrate doping concentration, as given in the legend. The solid lines are the experimental results from reference [5], and the dashed lines are the results obtained via the Monte Carlo simulator.

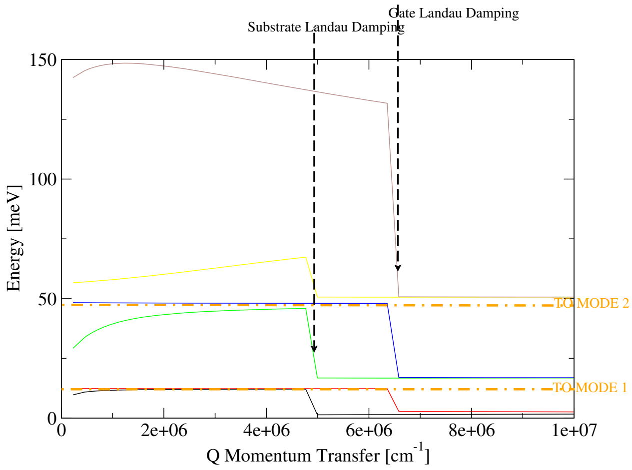

Fig. 2. Polaron dispersions considering Landau damping for the substrate and for the gate. The gate Landau damping is effective for higher momentum transfer since the doping is higher in that region.

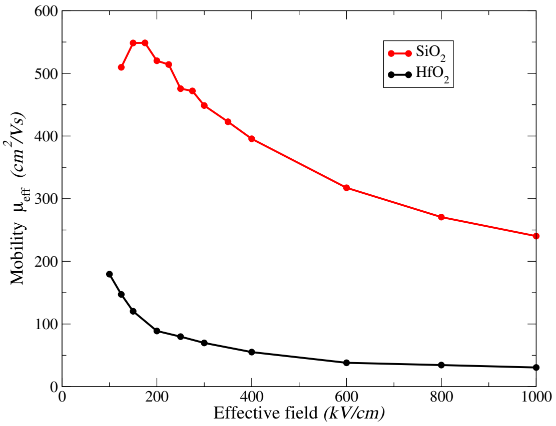

Fig. 3. Electron mobility in the inversion layer at 300 K versus effective field E_{eff}. The results reported are for HfO_2 and SiO_2, as shown in the legend.

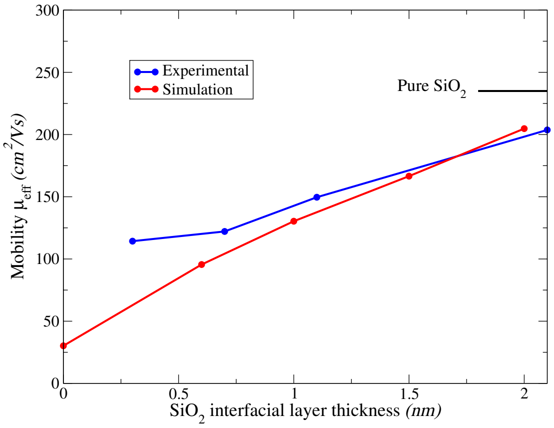

Fig. 4. Electron mobility in the inversion layer at 300 K as a function of the SiO_2 interfacial layer thickness, for a field E_{eff}=1000 $kV\,cm^{-1}$. As comparison is reported also the value for the mobility for pure HfO_2, corresponding to 0 nm layer thickness, and for pure SiO_2.

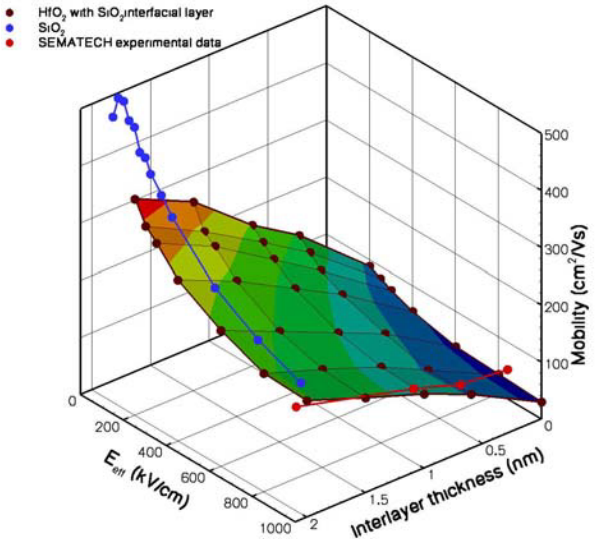

Fig. 5. Electron mobility in the inversion layer at 300 K for HfO_2 versus effective field E_{eff} and the SiO_2 interfacial layer thickness. The mobility for pure SiO_2 and the experimental results [3] are also reported.

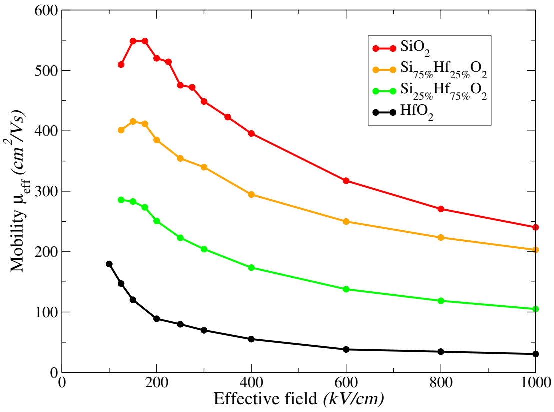

Fig. 6. Electron mobility in the inversion layer at 300 K versus effective field E_{eff} for an alloy of $Si_{1-x}Hf_xO_2$ as given in the legend.