Full-Band Particle-Based Simulation of 85 nm AlInSb/InSb Quantum Well Transistors

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ABSTRACT

Due to its high electron mobility at room temperature and its narrow band gap of 0.17 eV, Indium Antimonide (InSb) has a great potential for very low power and extremely high frequency applications. Previous simulations [1] on a high-speed 200 nm quantum well transistor described in [2] predicted very good performance in terms of cut-off frequency and bias requirements. However, the need for high integration scale implies smaller transistors, such as the sub 50 nm SOI MOSFETs demonstrated by Intel [3]. The design of such devices requires the implementation of efficient and accurate CAD tools.

In this work, we model and simulate an 85 nm AlInSb/InSb quantum well transistor by using a particle-based, full-band simulator based on the Cellular Monte Carlo (CMC) method [4], [5]. The geometry and doping profile of the simulated transistor are shown in Fig.1. The layout consists of a 160 nm unintentionally doped $Al_{0.2}In_{0.8}Sb$ substrate, a 20 nm thick InSb channel, a 5 nm thick spacer and a 45 nm thick $Al_{0.2}In_{0.8}Sb$ barrier. A δ-doped donor layer (1.3×10^{12} cm^{-2}) is located between the spacer and the barrier to increase the electron mobility. The transistor has an 85 nm gate length and a source to drain separation of 750 nm. Fig.2 shows the conduction band profile obtained with this layout. The quantum well where the charge transport occurs can be easily seen in the channel.

The InSb electronic band structure (Fig.3) used for the simulations is computed using the empirical pseudopotential method [6]. Momentum-dependant scattering rates are computed according to the work of Fischetti and Laux [7], and tabulated within the CMC framework, while the full phonon spectra are obtained with the 14-parameter empirical shell model [9]. Quantization effects are accounted for by using the effective potential technique [10].

The complete static and dynamic characterization of the simulated quantum well transistor as well as the noise analysis will be presented. The static and dynamic parameters, such as I-V curves or cutoff frequency (f_t) will be extracted showing all the advantages of the Indium Antimonide technology; the cutoff frequency will be compared with traditional Si MOSFET, technology and a comparison with recently published experiments [11] will be shown as well.

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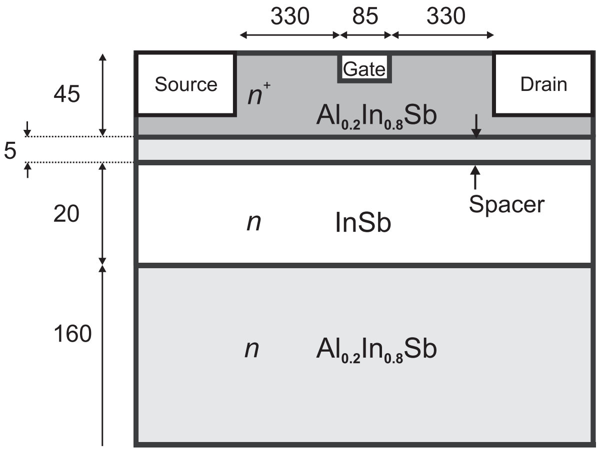

Fig. 1. Schematic layout of the simulated quantum well transistor. The dimensions are indicated in nm.

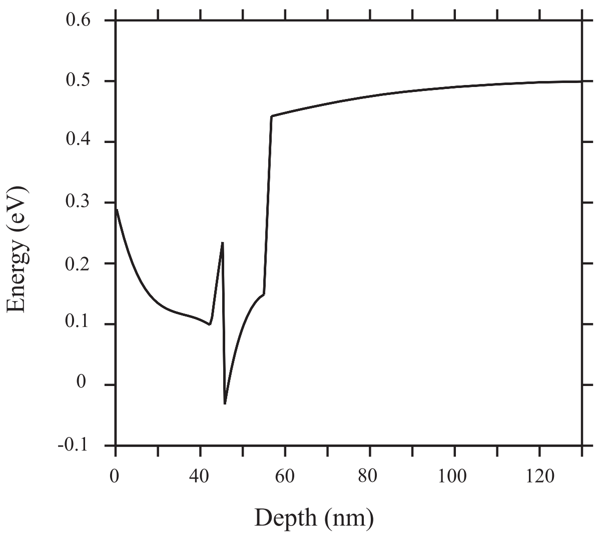

Fig. 2. Profile of the conduction band underneath the gate.

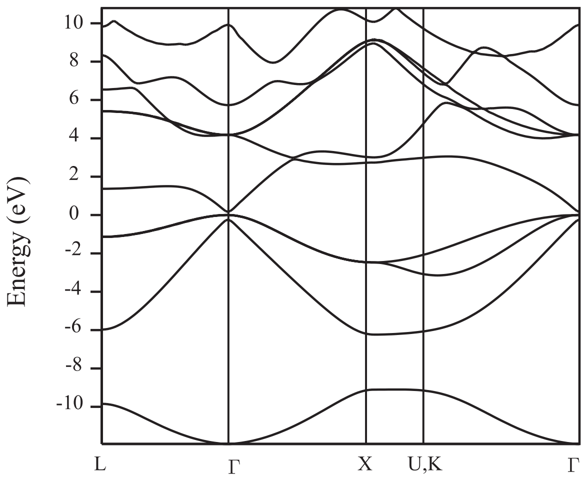

Fig. 3. Band structure of InSb computed using the empirical pseudopotential method.