11th International Workshop on Computational Electronics
TU Wien, 25-27 May 2006

Thermal Noise in Nanometric DG-MOSFET

P. Dollfus, A. Bournel, and J.E. Velázquez*
Institut d'Electronique Fondamentale, CNRS UMR 8622, Université Paris-Sud 11, F-91405 Orsay, France
*Dept. Física Aplicada, Universidad de Salamanca, E-37008 Salamanca, Spain
e-mail: js@usal.es

DESCRIPTION OF DEVICES AND MODEL

In nano-scale FETs, the fluctuations in the number and position of dopants in the channel makes necessary the use of a transport model including the atomistic nature of ionized impurities and 3D Poisson solver. These fluctuations induce spreading in overall device performance and should be reflected on noise characteristics. The present work deals with the study of thermal noise in Single-Gate Fully-Depleted SOI (SG) and Double-Gate (DG) MOSFET using self-consistent 3D Monte Carlo simulation including the effect of discrete impurities in the channel.

The atomistic approach describing the electron-ion interaction in the presence of discrete impurities was presented in [1]. This model has been successfully used to study the effect of impurity position in the channel of 50 nm bulk-MOSFETs [2]. The influence of atomistic doping on noise in nano-resistors has been tackled in [3].

The simulated devices (Figs. 1 and 2, where values L_G=25nm, L_{ch}=17nm, T_{Si}=5nm, T_{OX}=1.1nm, and W=15nm apply to both structures) consist of ultra-thin SG and DG transistors (denoted as SG1 and DG1, respectively). They operate at V_{DD}=1V. Source/channel and channel/drain junctions are assumed to be abrupt with continuous doping of 5×10^{19}cm^3 in S/D regions. We consider the possible presence of a single residual P type impurity in the channel of DGMOS.

RESULTS

Figures 3a and 3b show the typical effect of the presence of a single residual impurity on the transfer characteristics of both SG and DG MOSFET. We compare the case of channel without impurity (solid line) to the case of channel with one impurity in $X_I = 5.25$ nm (dashed line). In the case without impurity, the I_{on} current in DG1 (26µA) is only 40% higher than in SG1 ($I_{on} = 18.5$µA). This apparently good result for SG is only due to strong short-channel effects which induce high output conductance and also poor subthreshold behavior. The presence of a single impurity in the channel (dashed lines) perceptibly shifts the transfer characteristics and degrades I_{on}. This effect seems stronger in SG than in DG which is confirmed by Fig. 3b where the relative variation of I_{on} is plotted as a function of impurity position between X=0 and X=17 nm. The I_{on} degradation reaches 6% for DG and 10.5% for SG if the impurity is located near the source-end. An impurity located near the drain-end of the channel has a much smaller impact.

In order to evaluate the noise performance of both SG and DG transistors we first studied the current fluctuations for the same gate overdrive (V_{GS}=V_{DS}=V_{DD}). We considered three structures: SG1, DG1 and a DG with one P-type residual impurity located near the source (DG2 from now on). From Fig. 4 it follows that for the same gate overdrive the spectral density of the gate current (*Sigig(f)*) is considerably larger in SG1 than in both DG1 and DG2. In all the structures *Sigig(f)* exhibits the typical f^2 dependence and the slower increase with frequency for the DG structures must be attributed to a partial cancellation of the fluctuations due to the double gate topology. On the contrary, the SG exhibits the lowest value of the spectral density of the drain current (*Sidid(f)*) (Fig. 5). Preliminary calculations of noise figures point out a reduction of this key parameter in DG structures, in agreement with the observed behaviour of *Sigig(f)* and only little impact of the residual impurity (DG2). Further work is needed in order to extend the calculations to other regimes and fully establish if DG can effectively guarantee lower noise operation than SG ones and the weight of residual impurities in the channel.

REFERENCES

[1] S. Barraud, P. Dollfus, S. Galdin, P. Hesto, Solid-State Electron., **46**, 1061 (2002)
[2] P. Dollfus, A. Bournel, S. Galdin-Retailleau, S. Barraud, P. Hesto, IEEE Trans. Electron Dev., **51**, 749 (2004)
[3] P. Dollfus, J.E. Velázquez, A. Bournel, S. Retailleau, Proc. IWCE-10, J. Comput. Electron., **3**, 311 (2004)

ISBN 3-901578-16-1

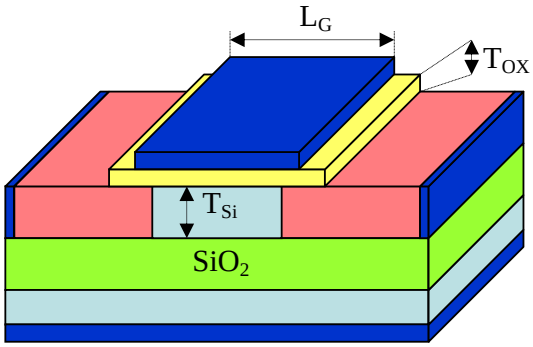

Fig. 1.a Schematic picture of the simulated SGMOS

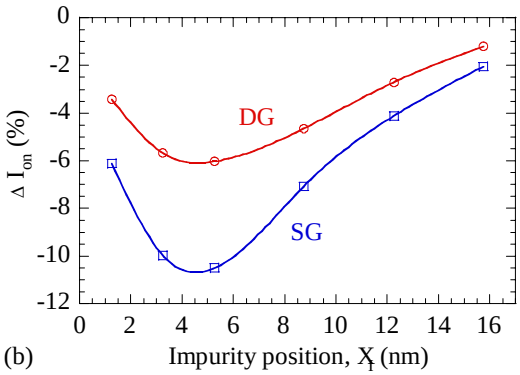

Fig. 3b. I_{on} versus lateral position X_I of a single impurity in the channel with respect to SG1 and DG1.

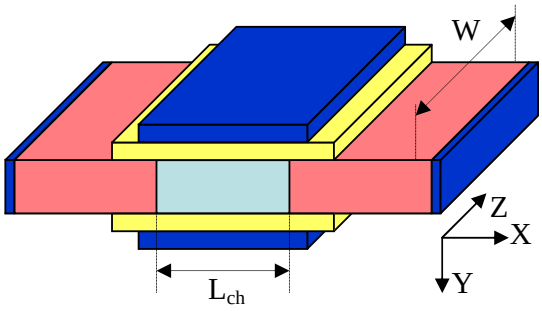

Fig. 2. Schematic picture of the simulated DGMOS

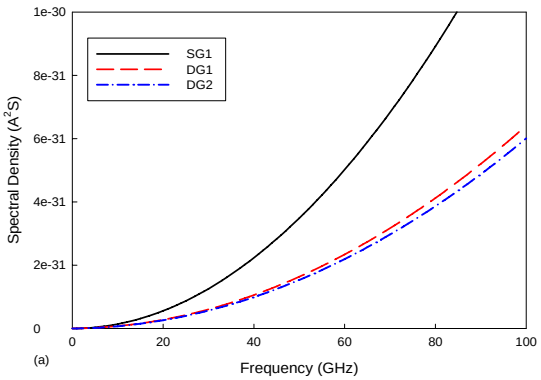

Fig. 4. $S_{igig}(f)$ at the same value of the gate overdrive

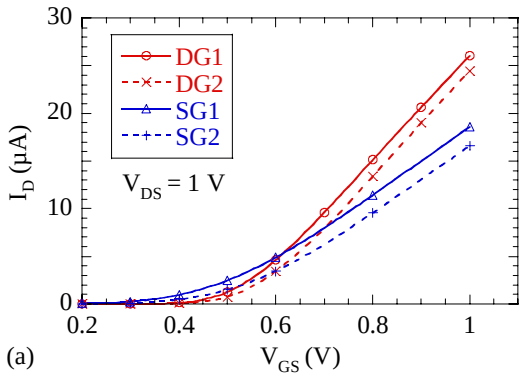

Fig. 3a. I_D-V_{GS} characteristics of SG and DG MOS.

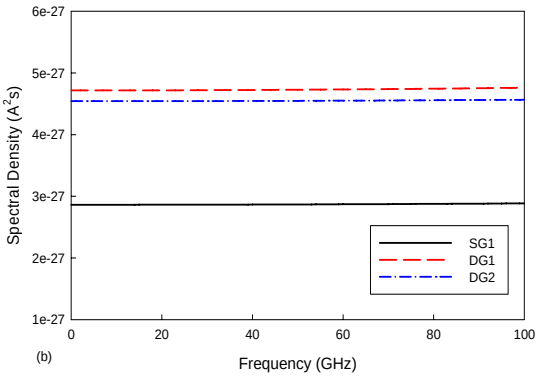

Fig. 5. $S_{idid}(f)$ at the same value of the gate overdrive