Negative Gate-Overlap in Nanoscaled DG-MOSFETs with Asymmetric Gate Bias

Xue Shao and Zhiping Yu
Institute for Microelectronics, Tsinghua University, Beijing 100084, China
E-mail: shaox97@mails.tsinghua.edu.cn

ABSTRACT

The transfer characteristics of double-gate (DG) MOSFETs are numerically simulated with 2D quantum drift-diffusion (QDD) model. Negative gate-overlap is introduced in devices to optimize the dynamic capacitance characteristics to get the best speed performance. Separate controlling of the back gate to vary the threshold voltage is investigated.

INTRODUCTION

DG-MOSFETs/FinFETs with ultra thin bodies are the way to suppress the DIBL and drain leakage when devices are scaled down below 50nm. Negative gate-overlap (Fig. 1) has been conceived to suppress drain leakage in literature [1-2]. But no dynamic performance has been studied. In this work, QDD model [3] (or density gradient model) is used to calculate the effects of quantum mechanics. A complete gate-S/D alignment can suppress short-channel effects (SCE) most but the gate capacitance is also the largest for fixed channel length and width. Applying an appropriate negative gate-overlap can optimize the device for best speed performance.

MODEL DESCRIPTION

A 2D numerical simulator Taurus-PMEI [4] was used to implement our simulation. All devices in this work are L_{ch}=10nm, W_{ch}=3nm and T_{ox}=2nm nMOSFET. S/D doping of device is 2.0e20/cm^3 and channel p-type doping is 1.0e17/cm^3. QDD model with Scharffeter-Gummel approach [5] was used. Constant carrier mobility is assumed. Fig. 2 plots the electron and current density distribution within the device from using both DD and QDD models. Apparently, electrons peak away from the Si/SiO$_2$ interface because of the quantum effects.

NEGATIVE GATE-OVERLAP

Negative gate-overlap weakens the gate control and increases the resistance under gate at on-state, but it reduces the gate capacitance. So there is a tradeoff between SCE control and device dynamic performance. Fig. 3 shows the I-V cures for different length of gate-overlap and Fig. 4 for C-V curves. The quantum effects affect not only the distribution of carrier and current densities but also capacitance. QM effects decrease capacitance and increase threshold voltage, especially for nanoscaled devices. To predict the speed performance of devices, we extract the I_{on}, I_{off} and dynamic capacitance using both DD and QDD models. Using the following delay time for characterizing the circuit speed,

$$t \approx \bar{C}_g V_{dd} / I_{on} \qquad (1)$$

Fig. 5. shows the trend of t vs. $L_{overlap}$. The device speed will increase about 20% when the gate-overlap changed from zero to -1.0nm.

BACK GATE CONTROL

Compared to the simultaneous control of front and back gates, it is more flexible to bias the back gate separately. Fig. 6 shows I-V curves for different V_{gb} bias. With higher V_{gb}, device works with lower threshold voltage. So the circuit speed is boosted benefited from the higher drain current. Lower V_{gb} makes the threshold voltage of devices higher. This decreases I_{on} and I_{off} greatly. So the circuit works with low-power dissipation. The results in Table 1 verified this prediction with QDD model. Note that, the power dissipation (PD) of the switching state refers to the average PD caused by gate charging/ discharging current at 1GHz. And the PD of On/Off state refers to the PD caused by channel current when the device switches between on/off states.

CONCLUSIONS

An appropriate negative gate-overlap improves circuit speed performance and also decreases power dissipation. Controlling the back gate separately is an appropriate way to make circuits adaptive for more versatile applications.

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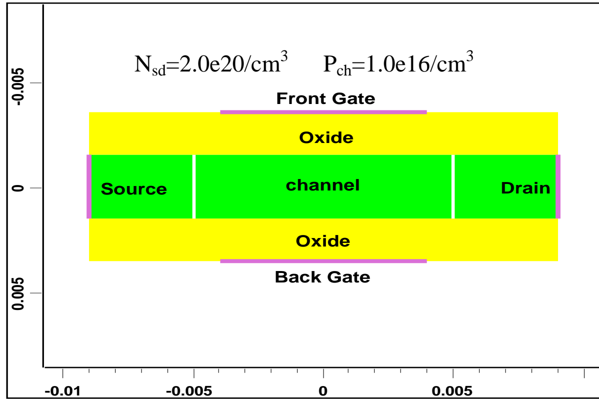

Fig. 1 Negative gate overlap DG-MOSFET structure

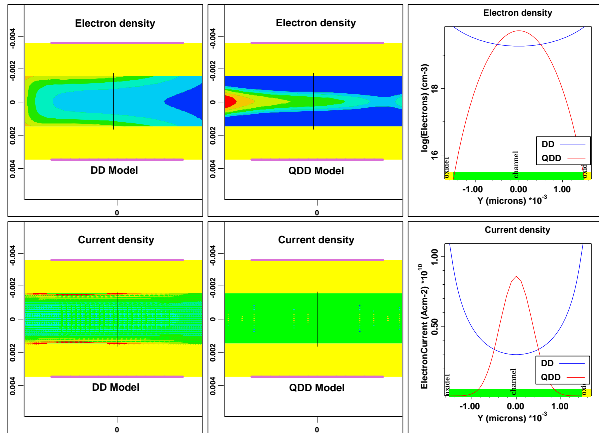

Fig. 2 Electron and current density in channel (V_{gs}=V_{ds}=1V)

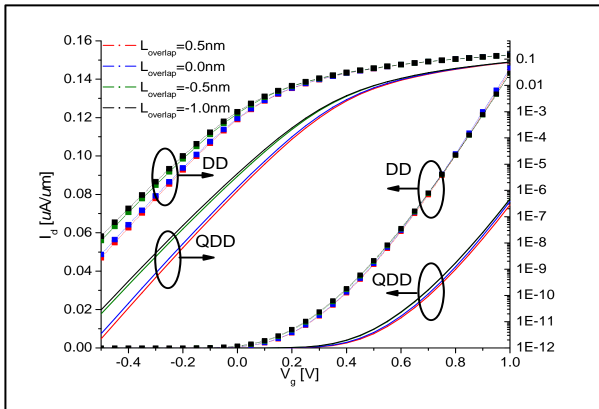

Fig. 3 I-V curves for 10nm-channel DG-MOSFETs (V_{ds}=1.0V)

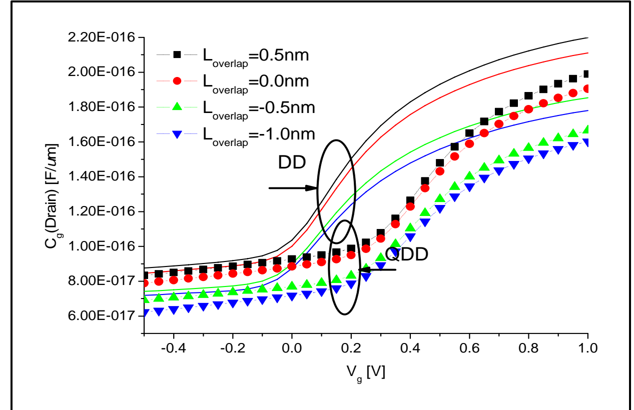

Fig. 4 C-V curves for 10nm-channel DG-MOSFETs (V_{ds} =1.0V)

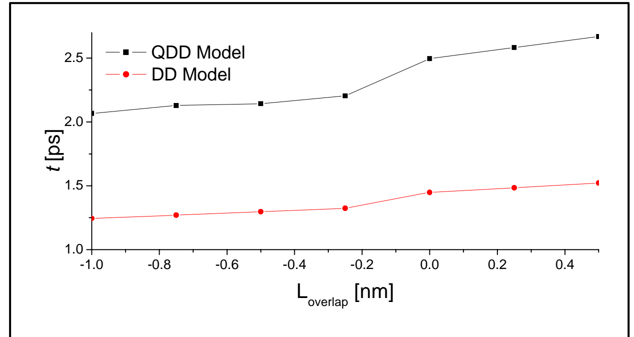

Fig. 5 Delay time of devices with different $L_{overlap}$

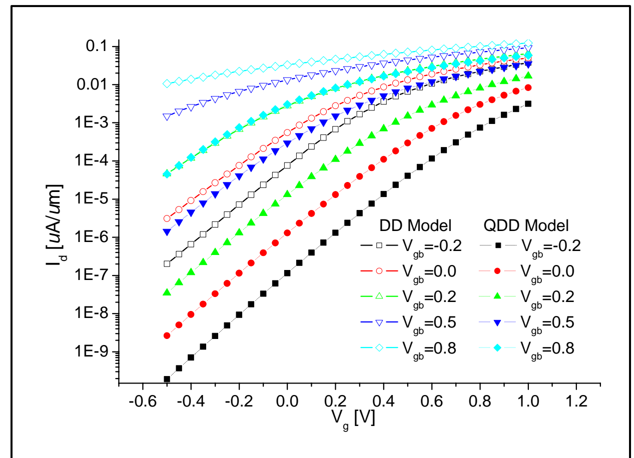

Fig. 6 I-V curves for 10nm-channel DG-MOSFET (fixed V_{gb})

V_{gb} (V)	Device parameter			Power dissipation (μw/μm)		
	V_{th} (V)	S_{sub} (mV/dec)	Delay (ps)	On state	Off state	Switch state*
-0.5	0.87	170	144	3.4e-4	2.7e-9	5.0e-2
-0.2	0.82	176	20	3.1e-3	1.2e-7	6.2e-2
0.0	0.75	181	8.6	8.4e-3	1.3e-6	7.2e-2
0.2	0.66	186	4.7	1.7e-2	1.3e-5	8.0e-2
0.5	0.50	198	2.5	3.5e-2	2.9e-4	8.7e-2
0.8	0.31	225	1.6	5.8e-2	3.0e-3	9.2e-2

Table 1 Device characteristics at 1GHz (V_{ds}=1.0V, QDD model)