A 3D parallel device simulator is employed to study the impact of charge fluctuations in the recess region of nanometre scale HEMTs. The simulator [1] is based on a drift-diffusion (D-D) approach using finite element discretisation on an unstructured tetrahedral mesh [2]. In order to reduce computational time, the simulator is parallelised via the MPI library. Fig. 1 shows the parallel efficiency obtained using the 3D D-D device simulator for the solution of Poisson’s equation at equilibrium using a mesh with 76500 nodes.

The intrinsic parameter fluctuations are expected to affect the RF performance and the matching of submicron HEMTs [3]. Random variations in the Si δ-doping and In content of the channel ternary alloy will induce significant parameter fluctuations in $I_D-V_G$ characteristics of 50 nm gate length InP HEMTs [3]. In this work we study the effect of interface charge fluctuations in the recess regions of HEMTs on device characteristics and compare it with the effect induced by charge fluctuations in the δ-doping layer and by variations in the ternary alloy content. Fig. 2 shows the difference between the electron densities at equilibrium for a 120 nm pseudomorphic InP HEMT. Figs. 5 and 6 compare $I_D-V_G$ characteristics at drain biases of 0.1 and 0.8 V respectively, for the 50 nm transistor. The effect of interface charge is smaller compared to the effect in the 120 nm PHEMT but the qualitative behaviour is similar. A statistical study of the effect of fluctuations in the discrete interface charge in the recess regions on the characteristics of both HEMTs will be reported at the conference.

**REFERENCES**


Fig. 1. Parallel efficiency for the solution of Poisson’s equation at equilibrium using a 76500 node mesh.

Fig. 2. Difference in electron density at equilibrium between a device with an interface charge of $-2 \times 10^{12} \text{cm}^{-2}$ in the recess layer and a device without the interface charge, in a plane along the 120 nm PHEMT InGaAs channel. The x-axis is along the device with the zero set in the middle of the gate and the y-axis is along the device width.

Fig. 3. $I_D$-$V_G$ characteristics at $V_D=0.1 \text{ V}$ for the 120 nm PHEMT. Full squares are for 3D D-D simulations with excluded interface charge and stars are for 3D D-D simulations with included interface charge. All simulations, including MC results, represent an intrinsic device. Experimental data are also shown for a comparison.

Fig. 4. $I_D$-$V_G$ characteristics at $V_D=1.0 \text{ V}$ for the 120 nm PHEMT. The symbols have the same meaning as in Fig. 3.

Fig. 5. $I_D$-$V_G$ characteristics at a low drain bias of 0.1 V for the 50 nm InP HEMT. The results obtained from the 3D D-D simulator with interface charge excluded (full squares) and included (stars), and MC results are shown, all for an intrinsic device. Experimental data given by open triangles are presented for a comparison.

Fig. 6. $I_D$-$V_G$ characteristics for the 50 nm InP HEMT. The same data from 3D D-D and MC device simulators as in Fig. 5 are shown but at a high drain voltage of 0.8 V.