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Strain Engineering with $Si_{1-y}C_y$ Source and Drain Stressors

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INTRODUCTION

To improve the Si-MOSFET performance, one attractive approach is to enhance carrier mobility and transistor drive current by using strain-induced effects. Recently, group IV alloys such as $Si_{1-x}Ge_x$ and $Si_{1-y}C_y$ have attracted great attention as new materials for introducing band gap engineering in Si technology. It has been shown that hole and electron mobility is considerably enhanced in a MOSFET by employing silicon–germanium (SiGe) stressors in the source and drain regions and nitride cap layer. Recently, a novel 50 nm gate length strained-Si n-MOSFET comprising $Si_{1-y}C_y$ S/D regions, metal gate and high-k gate dielectric has been demonstrated [1].

There is no experimental investigation on the lattice strain distribution in such a transistor structures. Understanding the strain distribution and its effect on the device performance will be important for channel strain engineering in CMOS transistors. In this paper, technology CAD (TCAD) approach is taken to explore the stress management in the SiC (S/D region) and the distribution of local strain components in the channel region. Some of the issues affecting the MOSFETs DC and AC characteristics due to the SiC induced strain in the channel has been studied using SILVACO VWF-simulation suite.

SIMULATION METHODOLOGY

SiGe source and drain stressors lead to lateral compressive strain and vertical tensile strain in the Si channel [2]. On the other hand, the SiC source and drain stressors give rise to lateral tensile strain and vertical compressive strain in the Si channel, an effect complementary to that of SiGe source/drain stressors and will enhance electron mobility in n-channel transistors. This gives rise to the SiC-strained-Si heterojunction which enables increased electron injection velocity at the source end.

The ATHENA process simulation framework from SILVACO was used for the process simulation by implementing preceding ideas. Typical device structures for process-induced strained-Si MOSFETs (with SiC in S/D) and subsequent stress contour, generated from the process simulation, is shown in Fig. 1a and 1b.

RESULTS AND DISCUSSION

To explore the device design parameters space for advance MOSFETs with elevated SiC S/D structure, Silvaco ATLAS device simulation tools was used. C-interpreter function has also been used to incorporate the mobility enhancement, SiC material parameter and strain mismatch models. Fig. 2 shows the simulated DC output characteristics of a n-MOSFET with SiC in S/D, at room temperature for a gate voltage variation from 0.5 to 2.5V. The sub-threshold characteristics simulated at 10, 50 and 100 mV is also shown in Fig. 3. A sub-threshold slope (SS) of 81.6mV/dec and V_{th} ~0.52 V is obtained from simulation. The frequency response of the SiC embedded (PSS) n-MOSFET was simulated in the common source configuration and the necessary figures of merit are calculated from the simulated S-parameter data. Fig. 4 shows the magnitude of current gain ([h21] in dB) versus frequency for PSS n-MOSFETs with 10/0.1 µm device, at nominal Vgs ~1V. The extrapolation of the plots displays an f_T of about 98 GHz and f_{max} ~470 GHz.

CONCLUSION

In conclusion, local lattice strain in transistor structures with SiC stressors in the S/D regions was investigated. This work will be useful for channel

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strain engineering in complementary metal-oxide-semiconductor transistors.

REFERENCES

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[2] A. R. Saha, S. S. Mahato, S. Chattopadhyay, and C. K. Maiti, *Process-Induced Strain Engineering Beyond 90 nm Technology Node*, IWPSD-2005, New Delhi, India, 2005

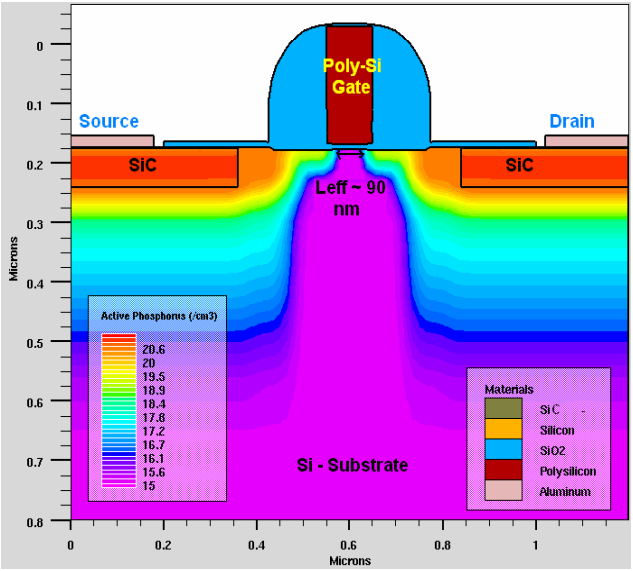

Fig. 1a. ATHENA simulated device structure

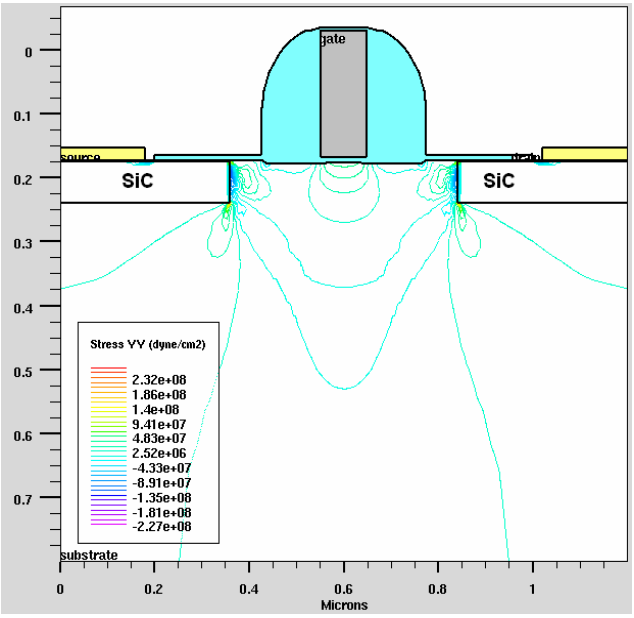

Fig. 1b. 2D Tensile Stress contours: indicating SiC induced strain

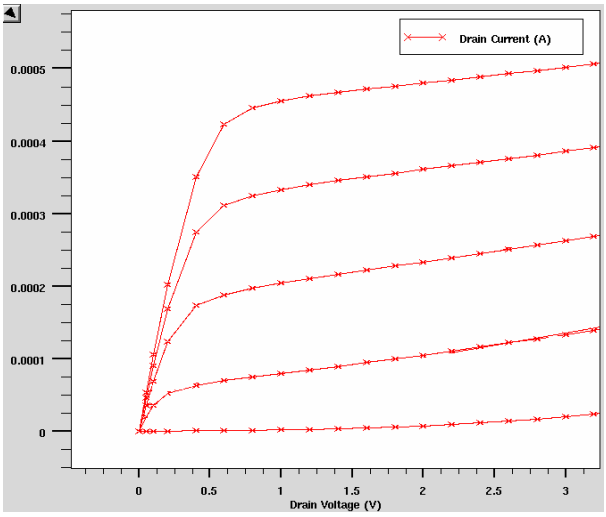

Fig. 2. Simulated DC output characteristics of SiC embebed (PSS) n-MOSFET structure with gate length (Lg~0.1 μm).

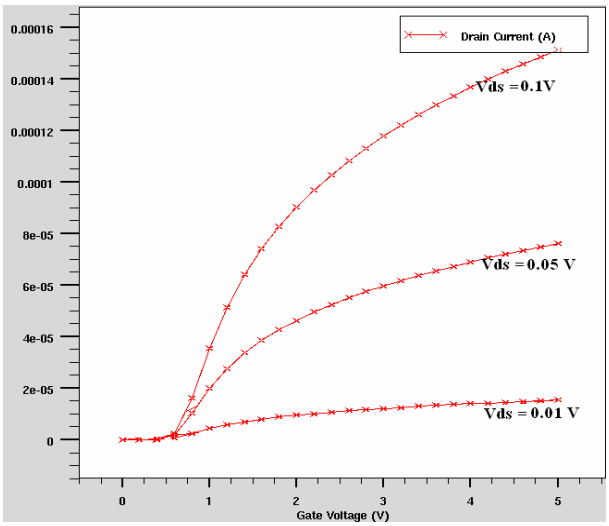

Fig. 3. Sub-threshold characteristics at different drain voltage.

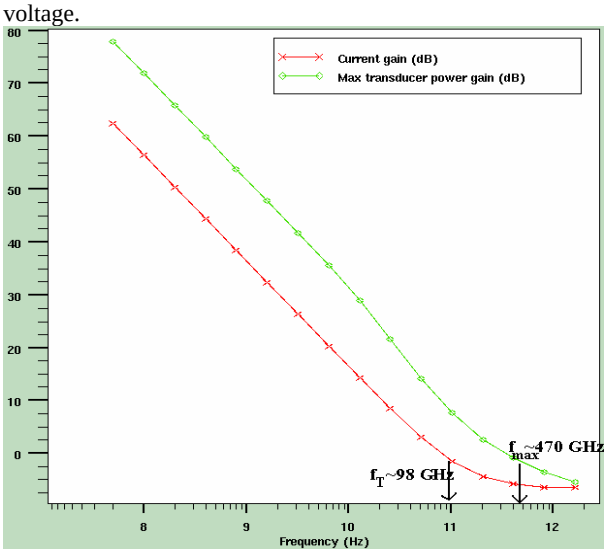

Fig. 4. Simulated Current Gain Vs frequency plot to extract the ac figure of merit.