A Simulation-Based Evolutionary Technique for Inverse Problems of Sub-65nm CMOS Devices

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ABSTRACT

In this paper, we utilize an evolutionary technique for inverse modeling problems of scaled-down 65 nm CMOS devices. The approach mainly bases upon the process and device simulations, evolutionary strategy, and empirical knowledge. For a set of given measured I-V curves of 65nm CMOS, a developed prototype performs the optimization task to automatically calibrate and inversely find out, for example the doping recipe and device physical model parameters. It benefits the development of fabrication technology and can be used for the performance diagnosis.

INTRODUCTION

The technology computer-aided design (TCAD) simulation has widely been used for the analysis of semiconductor devices [1]. For a set of given device's I-V curves, finding out the associated optimal configurations forms an inverse problem [2]. It nowadays plays an important approach to technology development as well as the performance diagnosis due to significant characteristic fluctuation of sub-65nm CMOS devices.

In this work, a simulation-based evolutionary system is developed for inverse problem of sub-65nm N- and P-MOSFET. Compared to realistic experimental process recipe, the achieved results demonstrate good extraction capability of the proposed method.

METHODOLOGY AND EXTRACTED RESULTS

Figure 1a shows the computational flowchart of the TCAD simulation-based inverse modeling problem. The developed system, shown in Fig. 1b, is mainly relying on a hybrid genetic algorithm (GA) [3] incorporating with other optimization techniques. Inset of Fig. 2 is a 2D cross-section view of the simulated 65 nm MOSFET with LDD doping profile. Table 1 shows the partial list of LDD profile parameters for process simulation, and physical model parameters for device simulation. Figure 2 shows the target I-V curves to be optimized and several most concerned physical quantities empirically. Figure 3 depicts the performance of three different calibration strategies. The single optimization approach is limited and can not improve the accuracy of extraction. It is necessary to perform process and device simulation simultaneously. The extracted curves are shown in Fig. 4 for both N- and P- MOSFETs, where Fig. 5 illustrates the inversely calibrated doping profile for the 65nm MOSFETs. A set of inversely optimized results is shown in Table 1.

CONCLUSIONS

We have presented an evolutionary system for inverse problem and tested on 65nm CMOS devices. Process and device parameters have been obtained according to realistic device data. The proposed system is now under developed to explore asymmetric transport phenomena due to fluctuation of source and drain implantations.

ACKNOWLEDGEMENT

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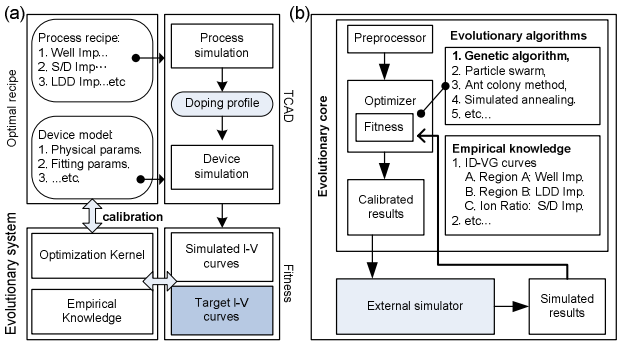

Fig. 1. (a) A flowchart of the proposed optimization system to solve the device inverse modeling problem. (b) An architecture of the developed system. The system has its built-in 2D/3D device and process simulation programs; it also interfaces to well-known TCAD tools.

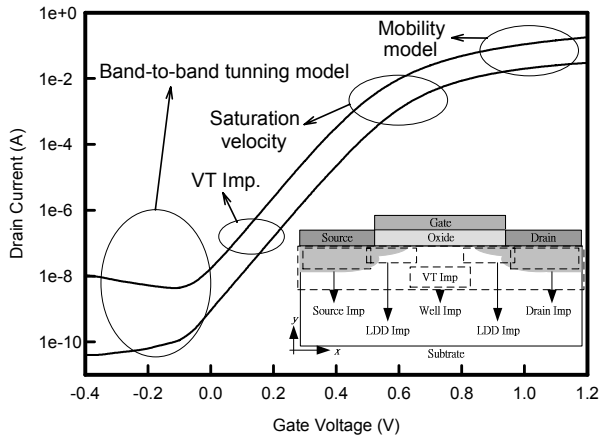

Fig. 2. An illustration of the target I-V curves to be extracted and empirical knowledge. The inset plot is a 2D cross-section view of the simulated MOSFET with LDD doping profile.

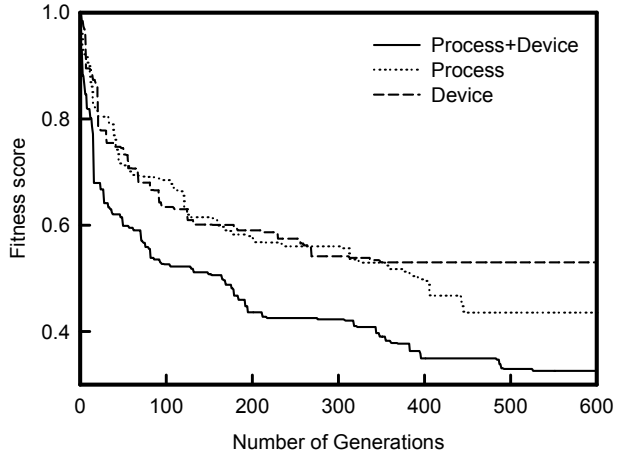

Fig. 3. The performance comparisons among three different evolutionary strategies. There are totally 31 process and device parameters to be optimized in the case of process and device simulations. The total time is about 70 hours on a PC-based Linux cluster with 16 CPUs.

Table 1. A partial list of process and device's parameters to be extracted for the explored 65nm N- and P-MOSFETs. The Schenk model [4] is adopted to describe the band-to-band tunneling. The enhanced Lombardi model [5] is selected as a mobility model.

Process Recipe	Parameter Range	Calibrated Result	
		N-MOS	P-MOS
Well Imp.	Energy: 300~500 KeV	462	276
	Dose: 5e12~5e13 cm^{-2}	2.6e13	3.1e13
LDD Imp.	Energy: 10~50 KeV	30	25
	Dose: 5e12~5e13 cm^{-2}	3.7e13	2.1e13
S/D Imp.	Energy: 20~80 KeV	17	11
	Dose: 1e13~1e14 cm^{-2}	2.1e13	1.5e13
Device Model	**Parameter Range**	**Calibrated Result**	
		N-MOS	P-MOS
Mobility model	B(cm/s): 2e7~8e7	462	276
	C($cm^{5/3}/V^{2/3}s$): 1e2~5e2	2.6e13	3.1e13
Velocity saturation model	Vsat_0(cm/s):1e6~1e8	9e6	8.1e6
	Vsat_exp: 0.5~1.0	0.81	0.94

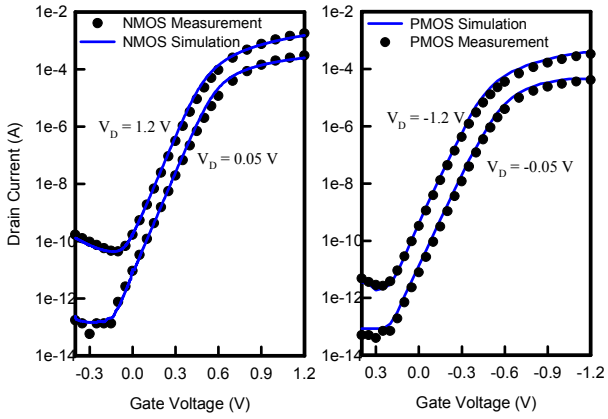

Fig. 4. The achieved accuracy of the extracted I-V curves for N- and P-MOSFETs, where gate length L = 65nm and device width W = 1μm. Results are simultaneously obtained with considering device and process configurations. Symbols are measured data and lines are eventually optimized result.

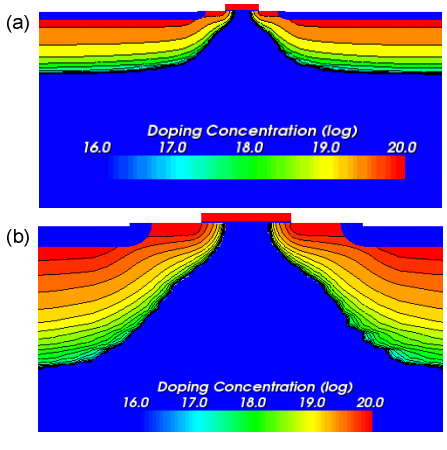

Fig. 5. The extracted 65nm (a) N-MOSFET doping profile and (b) a zoom-in plot of the profile. Similar results are obtained for the P-MOSFET. These results are corresponding to the optimized I-V curves shown in Fig. 4. We note that simulations are performed with 2D process and device structures.