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Simulation of Slow Current Transients and Current Compression in AlGaAs/GaAs HFETs

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INTRODUCTION

Compound semiconductor FETs, such as GaAs MESFETs, HFETs and GaN-based FETs, are very important devices for microwave power devices and ICs that are now receiving great attention, particularly for mobile communication applications. However, slow current transients are often observed even if the drain voltage V_D or gate voltage V_G is changed abruptly. This is called drain lag or gate lag [1]. Hence the dc *I-V* curves and ac *I-V* curves become quite different, resulting in lower ac power available than that expected from dc operation. This is called power (current) compression [2,3]. These are serious problems and there are many experimental works reported on these phenomena, but only a few theoretical works are reported for HFETs [4], although several numerical analyses were made for MESFETs [5,6]. Also, the lag phenomena were studied by changing only V_D or V_G. But both voltages should be changed during turn-on or RF drive. Therefore, in this work, we have made transient simulations of AlGaAs/GaAs HFETs, and particularly calculated cases when both V_D and V_G are changed abruptly, and derived quasi-pulsed *I-V* curves. As a result, we have clearly shown that the current compression could occur both due to substrate traps and surface states.

PHYSICAL MODEL

Fig.1 shows a modeled AlGaAs/GaAs HFET. As a substrate, we consider undoped semi-insulating GaAs where deep donors "EL2" (N_{EL2}) compensate shallow acceptors (N_{Ai}) [5]. As a surface state, we consider an acceptor-type state, and vary its energy level E_{SA} as a parameter because the detailed information is not obtained for AlGaAs surface. Basic equations are Poisson's equation including ionized deep-level terms, continuity equations for electrons and holes which include carrier loss rates via the deep levels, and rate equations for the deep levels.

SUBSTRATE-TRAP EFFECTS

Fig.2 shows calculated drain-current responses of the AlGaAs/GaAs HFET when V_D is changed abruptly from 0 V (V_{Dini}) to V_{Dfin} while keeping V_G at 0 V. Here, surface states are not included. The drain currents overshoot the steady-state values, because electrons are injected into the substrate, and the substrate trap (EL2) needs certain time to capture these electrons. Fig.3 shows the case when V_D is lowered abruptly from 5V to V_{Dfin} while keeping V_G at 0 V. The drain currents remain at low values for some period, and begin to increase slowly, showing drain-lag behavior. It is understood that the drain current begin to increase when the deep donors begin to emit electrons.

We have next calculated a case when both V_D and V_G are changed from an off point. Fig.4 shows calculated turn-on characteristics when V_G is changed from the threshold voltage V_{th} to 0 V. The off-state drain voltage V_{Doff} is 5 V, and the parameter is an on-state drain voltage V_{Don}. The characteristics are similar to Fig.3, and hence the change of V_D (drain lag) is essential in this case, although slight transients are seen when only V_G is changed (V_{Don} = 5 V in Fig.4). Fig.5 shows I_D-V_D curves. Here, we plot by point (x) the drain current at 10^{-6} s after V_G is switched on. This is obtained from Fig.4, and this curve corresponds to a quasi-pulsed *I-V* curve with pulse width of 10^{-6} s. (For reference, we also plot other quasi-pulsed *I-V* curves when only V_D is changed, which reflect the overshoot and undershoot). The drain currents in the pulsed *I-V* curve are rather lower than those in the steady state. This clearly indicates that the current compression could occur due to the substrate-trap effects, and it occurs due to drain lag in this case.

SURFACE-STATE EFFECTS

Next we have calculated a case when only the surface states are included. It is found that the lags are not seen when the energy level of deep-acceptor surface state E_{SA} is far from the valence band and it acts as an electron trap. The lags become important when the deep acceptor acts as a hole trap. Fig.6 shows calculated I_D-V_D curves for such a case. The current compression is significant, as shown by point (x), and it occurs mainly due to the change of V_G (gate lag) in this case.

COMBINED EFFECTS OF SUBSTRATE AND SURFACE

Finally, we have studied the case when both the substrate traps and surface states are included. Fig.7 shows an example of calculated I_D-V_D curves. It is seen that the lags (overshoot and undershoot) and current compression are very pronounced when comparing with Figs.5 and 6. This significant combined effect is an interesting feature which has not been pointed out.

REFERENCES

[1] S. C. Binari, P. B. Klein and T. E. Kazior, Proc. IEEE, vol.90, pp.1048-1058 (2002)
[2] R. E. Leoni et al., IEEE Trans. Electron Devices, vol.47, pp.498-506 (2000).
[3] U. K. Mishra, P. Parikh and Y.-F. Wu, Proc. IEEE, vol.90, pp.1022-1031 (2002).
[4] G. Verzellesi et al., IEEE Trans. Electron Devices, vol.50, pp.1733-1740 (2003).
[5] Y. Kazami, D. Kasai and K. Horio, IEEE Trans. Electron Devices, vol.51, pp.1760-1764 (2004).
[6] K. Horio et al., J. Appl. Phys., vol.98, no.12 (2005).

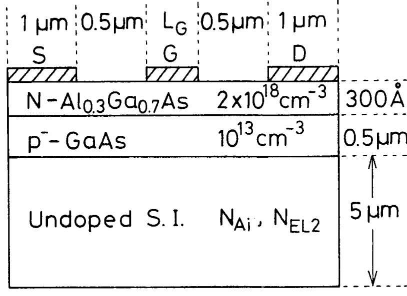

Fig.1. Device structure analyzed in this study

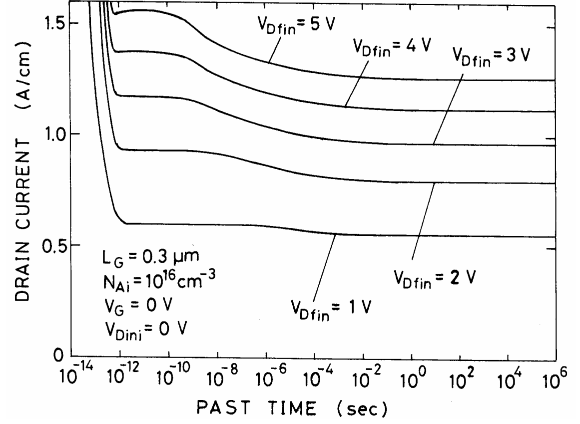

Fig.2. Calculated drain-current responses of AlGaAs/GaAs HFET when V_D is raised from 0 V to V_{Dfin}. V_G is kept 0 V.

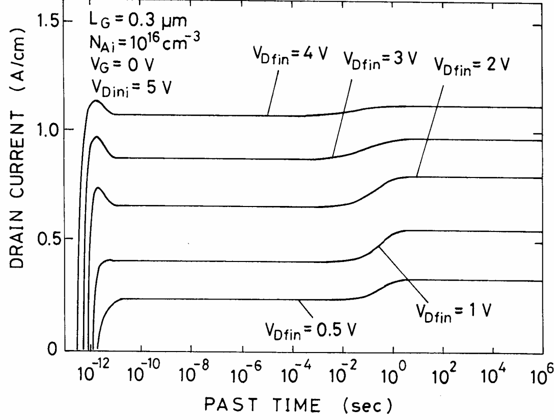

Fig.3. Calculated drain-current responses of AlGaAs/GaAs HFET when V_D is lowered from 5 V to V_{Dfin}. V_G is kept 0 V.

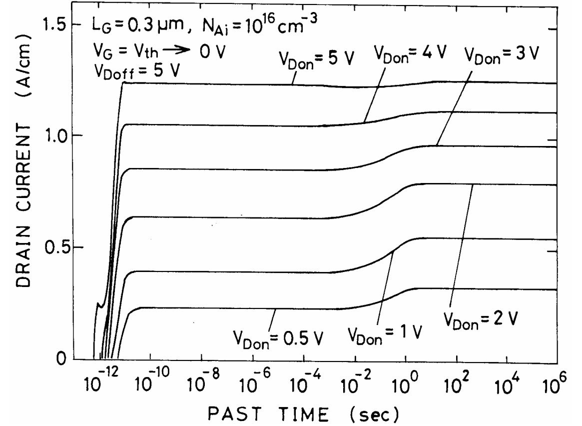

Fig.4. Calculated turn-on characteristics of AlGaAs/GaAs HFET when V_G is changed from V_{th} to 0 V. V_D is also changed from 5 V to V_{Don}.

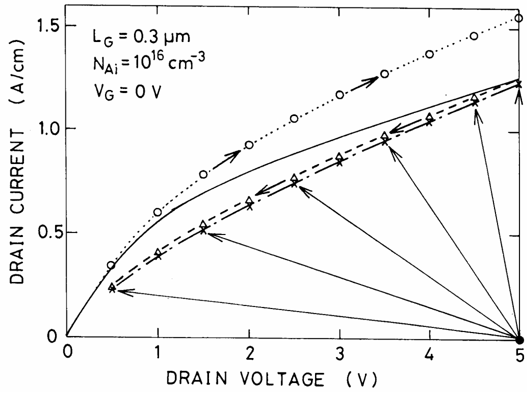

Fig.5. Steady-state I_D-V_D curve (solid line) and quasi-pulsed *I-V* curves of AlGaAs/GaAs HFET with a semi-insulating substrate. (x): V_{Goff} = V_{th} and V_{Doff} = 5 V (t = 10^{-6} s; Fig.4), (○): V_{Dini} = 0 V and V_G = 0 V (t = 10^{-9} s; Fig.2), (Δ): V_{Dini} = 5 V and V_G = 0 V (t = 10^{-6} s; Fig.3).

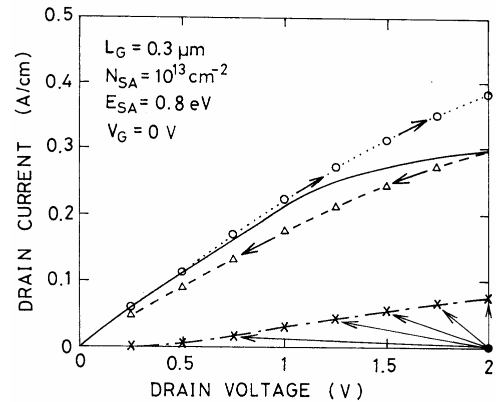

Fig.6. Steady-state I_D-V_D curve (solid line) and quasi-pulsed *I-V* curves (pulse width of 10^{-6} s) of AlGaAs/GaAs HFET with surface states but without substrate traps. (x): V_{Goff} = V_{th} and V_{Doff} = 5 V, (○): V_{Dini} = 0 V and V_G = 0 V, (Δ): V_{Dini} = 5 V and V_G = 0 V.

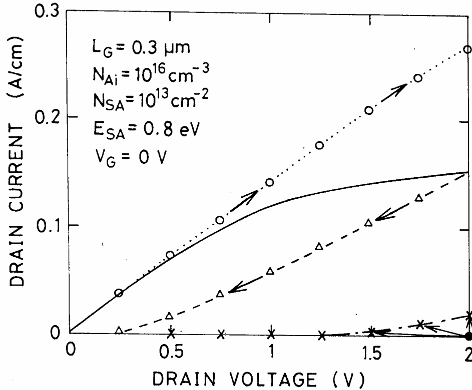

Fig.7. Steady-state I_D-V_D curve (solid line) and quasi-pulsed *I-V* curves (pulse width of 10^{-6} s) of AlGaAs/GaAs HFET with both surface states and substrate traps. (x): V_{Goff} = V_{th} and V_{Doff} = 5 V, (○): V_{Dini} = 0 V and V_G = 0 V, (Δ): V_{Dini} = 5 V and V_G = 0 V.