Efficient Full-Flow Process Simulation for 3D Structures including Stress Modeling

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MOTIVATION

As silicon based devices become smaller in size, conventional simulation methods using 2D structures become insufficient. Many effects, such as narrow width effect and line edge roughness require 3D simulation. Moreover, many new devices such as FinFET are 3D by nature. Also, many modern devices are built using stress engineering, which requires 3D stress modeling to predict device performance.

However, 3D process simulation is by its nature more complicated than 2D simulation and even with modern computers it requires a long simulation time. New methods are needed to perform 3D full-flow simulation in a reasonable amount of time.

HYBRID APPROACH

3D geometry modifications such as deposition, etch, oxidation and epitaxy, present a big challenge to traditional TCAD tools when performed with methodologies such as string algorithm or level-set movement, as these methodologies work only on a mesh. The most efficient method for performing such steps is using a solid modeling. However, solid modeling tools cannot perform process simulation steps, such as diffusion or implantation. A hybrid method, where etching, deposition and epitaxy steps are performed with a solid modeling tool, such as Synopsys' Sentaurus Structure Editor (SDE) and the diffusion and implantation steps are performed by a process simulator, such as Sentaurus Process (Sprocess) had been devised previously [1].

The hybrid method requires of segregation of the input flow into an SDE flow and Sprocess flow, which need to be manually intertwined. A new input flow definition strategy has been developed, which allows for keeping the process flow in one single file, and letting the interpreter to do the necessary book keeping while switching between the tools.

The methodology works in two modes of meshing strategy, called remesh every switch and paint by number. In the former, entirely new mesh is built at every switch. In the latter case, all steps from the full flow are combined into one structure and the merged regions are assigned numbers. The mesh is built once on the merged structure and regions indicated by numbers change material type to obtain the structure at a particular step.

STRESS MODELING

Solving for stress-strain equations concurrently with diffusion equations slows down simulation time considerably. To avoid this, we run the process simulation twice: Once solving only for implantation steps and diffusion equations and a second time only solving the mechanical equations. The second run is extremely fast compared to the first one, since the simulator can choose large time steps. The results are then combined to perform device simulation including stress effects on band gap and mobility.

CONCLUSION

The methods described have been applied to several 3D process flows, including a FinFET [2], a CMOS image sensor, a PMOS device with raised SiGe S/D and other structures. The simulation times are about an order of magnitude faster than using a process simulator with a mesh to perform the topography modification steps. This makes 3D simulation feasible for everyday use.

REFERENCES

[1] "*More Efficient Process Flow for 3D NMOS Transistors*", Synopsys TCAD News, October 2004. http://www.synopsys.com/products/tcad/pdfs/news_oct04.pdf
[2] M. Nawaz, P. Haibach, E. Landgraf, W. Rösner, M. Städle, H. Luyken and A.H. Gencer "*Full 3D Process and Device Simulation for FinFET Optimization*", ISDRS 2005.

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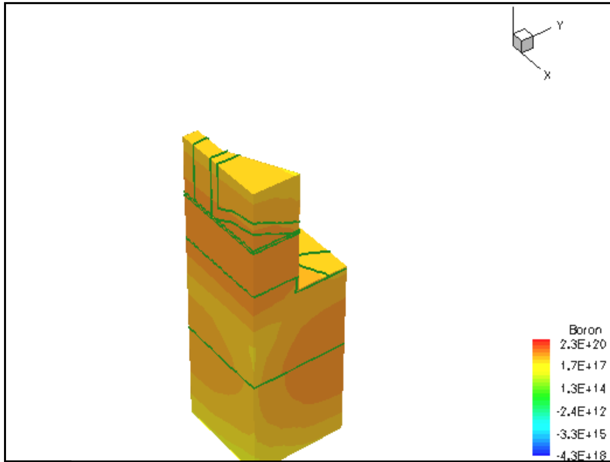

Fig. 1a. FinFET structure after fin formation. Note region boundaries from the merged structure.

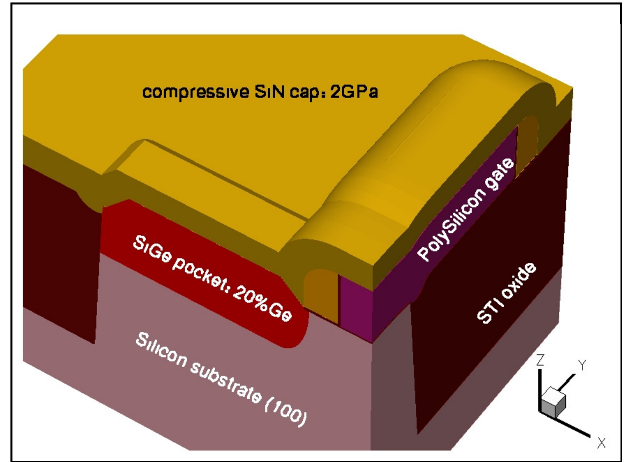

Fig. 3a. Final topography for SiGe raised S/D PMOS

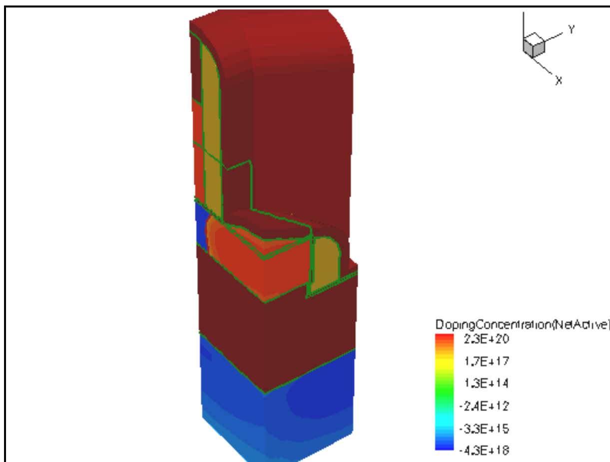

Fig. 1b. Final FinFET structure. Only one quarter of the FinFET was simulated to take advantage of symmetry.

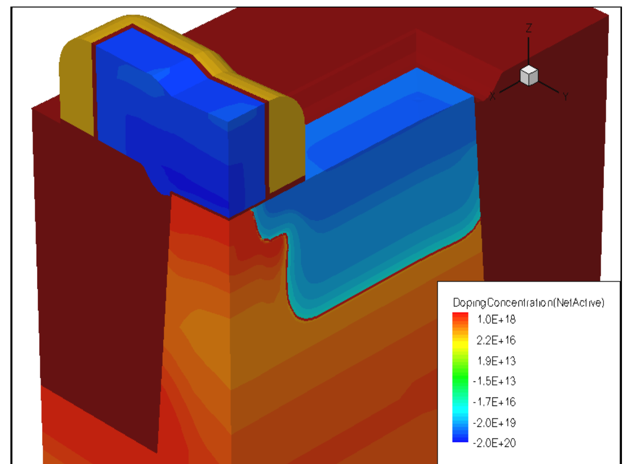

Fig. 3b. Final doping distribution for the 3D PMOS

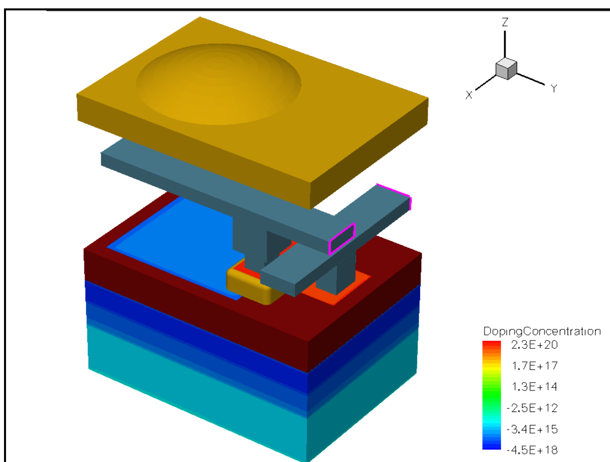

Fig. 2. Final topography for the CMOS image sensor

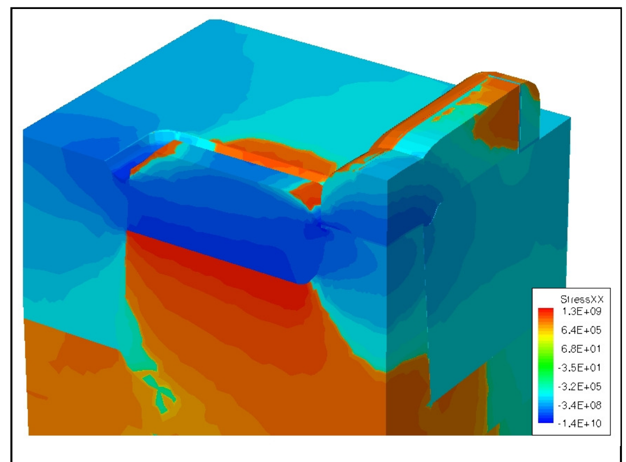

Fig. 3c. Final stress distribution for the 3D PMOS