Intrinsic Parameter Fluctuations due to Random Grain Orientations in High-κ Gate Stacks

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As the scaling of MOSFETs continues the requirement to maintain electrostatic integrity dictates an aggressive reduction of the oxide thickness below 1 nm, introducing intolerably high gate leakage [1]. This has led to the introduction of high-κ materials in the gate stack offering the required SiO_2 equivalent oxide thickness at increased physical thickness and reduced gate leakage. There are many technological issues [2] associated with the use of high-κ material in the MOSFET gate stack leading to mobility degradation. Some of these factors [3] will also introduce intrinsic parameter fluctuations in the corresponding MOSFETs, similar to the fluctuations introduced by random discrete dopants and oxide thickness variations. We recently reported an investigation of intrinsic parameter fluctuations in decananometre MOSFETs introduced by non-uniformity of the dielectric properties of the high-κ material due to *phase separation* of Hf and Si oxides [4]. Here we present a simulation study of another source of non-uniformity, also due to the polycrystalline nature of the high-κ dielectric material, which is *random grain orientation*. Each crystalline grain within the gate stack can have a random orientation which, due to anisotropy in the dielectric constant, leads to localised variations in gate-to-channel capacitance. This results in local fluctuations in the MOSFET surface potential leading to variations in characteristics from one device to the next. The possible granular nature of a high-κ film structure is illustrated in Fig 1 which shows a plan-view TEM image of a polycrystalline HfO_2 film, with different grain orientations.

The simulations were carried out with the Glasgow 'atomistic' device simulator, which has been modified to include a polycrystalline high-κ gate stack with variations in dielectric constant for different grains. In order to introduce a realistic grain structure a large AFM image of polycrystalline grains [5] has been used as a template. The grain boundaries in this image were traced in Adobe Illustrator and each grain was coloured to allow differentiation, as shown in Fig. 2. The image was scaled so that the grain diameters are in the range of 2-10nm (see Fig. 3), typical for a high-κ film [6].

The simulator imports a random (in both location and orientation) section of the grain template which corresponds to the dimensions of the device, and for each different grain assigns a dielectric constant chosen randomly from within a given range. An example is shown in Fig. 4. The resultant fluctuations in surface potential are shown in Fig. 5.

Fig. 6 shows the fluctuations in threshold voltage, σV_T, for bulk MOSFETs scaled from 50nm to 15nm. The gate stack for each device consists of a 0.5nm interfacial SiO_2 layer with the polycrystalline high-κ dielectric above. One would expect that as the device dimensions are reduced the magnitude of the fluctuations would increase, however this is tempered by the necessary scaling of oxide thickness which reduces the capacitative contribution of the high-κ relative to the interfacial layer, limiting the effect of the dielectric fluctuations.

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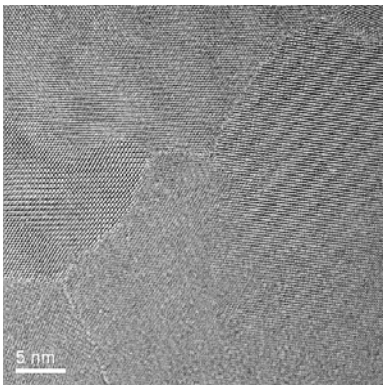

Figure 1. Top view TEM image of a HfO_2 film showing different polycrystalline grains each with different crystalline orientation.

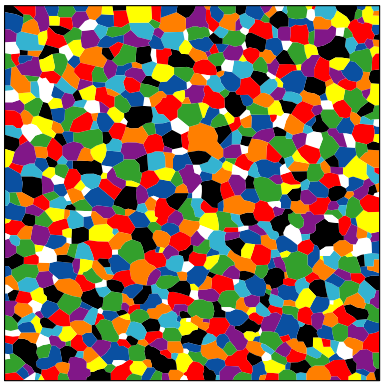

Figure 2. An AFM image is used as a template in Adobe Illustrator where the grain boundaries are traced and filled with colours. It is important to note that the colours used in this image are purely to allow the simulator to differentiate between different grains and bear no relation to the dielectric constant assigned to that grain by the simulator.

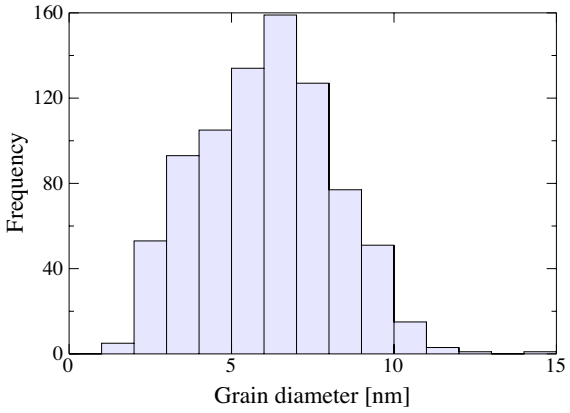

Figure 3. The grain image is scaled so that the grain diameters are between 2 and 10 nm [6]. The diameter is calculated from the area of the grain assuming a circular grain shape. The image file is then written in a format readable by the simulator at a particular resolution, e.g. 1 pixel/nm.

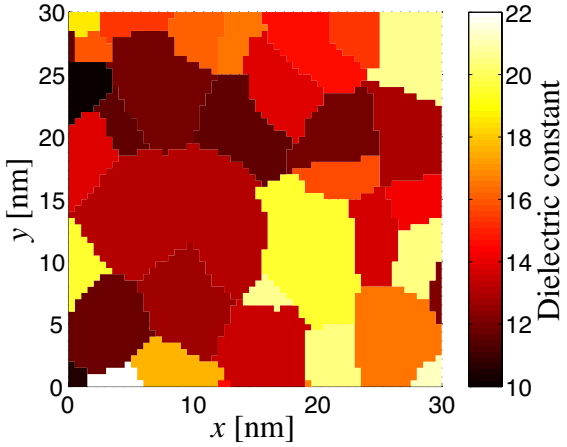

Figure 4. Once a randomly selected region of the grain image is imported to the simulator a recursive spatial search algorithm is used to identify every grid node within a particular grain and assign the dielectric constant for that grain to all those nodes. The dielectric constant is chosen randomly from within a given range. Here is shown an example for a 30×30nm channel MOSFET.

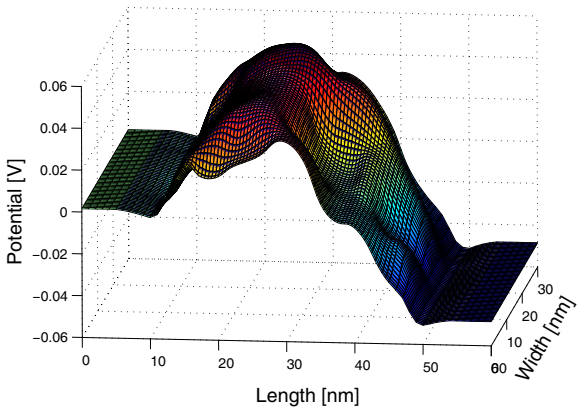

Figure 5. Surface potential in a 30×30nm MOSFET demonstrating the fluctuations induced by variations in dielectric constant.

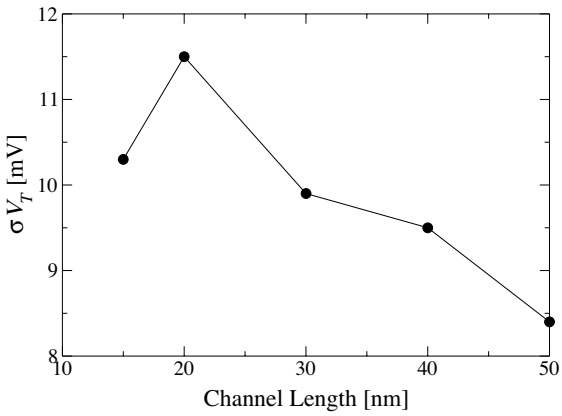

Figure 6. σV_T for bulk MOSFETs scaled from 50nm to 15nm. Simulations of 200 devices with unique grain pattern and associated dielectric constants were performed for each channel length.