Influences of Grain Structure on Thermally Induced Stresses in 3D-IC Inter-Wafer Vias

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We discuss the status of our thermo-mechanical modeling effort to provide parameters for the design and fabrication of 3D ICs based on benzocylcobutene (BCB) bonding (see Fig. 1). Broadly speaking, the stability concerns for inter-wafer Cu vias in 3D ICs are the same as for Cu-based MLM structures. For 3D ICs, a major reliability concern is the stability of the vias, which pass through several materials/layers. We are studying thermo-mechanical issues in these structures to help understand potential failure mechanisms.

In previous reports [2, 3], we describe our use of FEMLAB (COMSOL [4]) in thermo-mechanical modeling of inter-wafer Cu vias. Fig. 2 shows a schematic of a via through multiple layers; for details, see Refs. 2 and 3. The Cu was treated as a homogeneous material; the impact of grain size was introduced via correlations to copper yield stress, per Hall-Petch. We concluded that the inter-wafer Cu vias may fail due to the high stresses generated, depending upon details such as the diameter and pitch of the vias, and the BCB thickness. Our approach was validated by comparing results to data from reliability studies of Cu via structures in SiCOH and SiLK [5,6], and XRD studies of damascene-patterned Cu lines [7]. Because our results indicate that stresses will limit design space, it is important to refine our computations to improve our predicted design parameters.

Our thermo-mechanical modeling results show large gradients in the principle stresses (*e.g.,* see Fig. 3). These stresses provide driving forces for Cu migration and failure, and motivates including Cu grain structure in the models. We have developed a finite element model (FEM) that includes the grain structure of the Cu vias. We use anisotropic elastic constants, taken from the literature, of individual Cu grains in via structures. We have generated randomly textured 3D grain structures, for demonstration purposes, and used COMSOL to perform thermo-mechanical modeling (see Fig. 4). The materials' properties and other model details can be found in Refs. 2 and 3. Stresses are those induced by a temperature change from a stress-free state at 523 K to 298 K.

We wrap up with a discussion of how PLENTE [8, 9], the code we use to represent and track grain structures, is combined with COMSOL. PLENTE uses level sets on finite elements to track the motion of multiple materials or multiple phases/grains in a 3D environment (see Fig. 5). Evolution can be due to deposition, etch, annealing processes, and/or be stress-induced and/or current-induced migration. In this study, PLENTE provides 3D grain structures to COMSOL, and COMSOL computes the forces acting on the grains. These forces are converted into grain boundary motion. PLENTE then updates the grain structure and the cycle is repeated. We will detail a novel method to extract a consistent structure for finite element analysis, after evolution.

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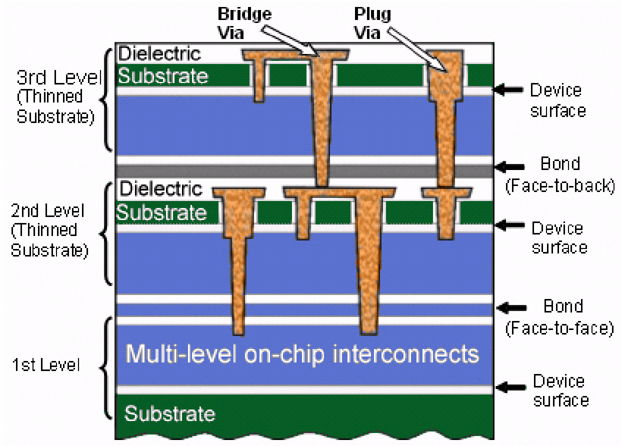

Fig. 1. 3D chip cross-sectional structure using "face-to-face" BCB bonding [1]. This schematic shows three wafers (2 BCB bond layers).

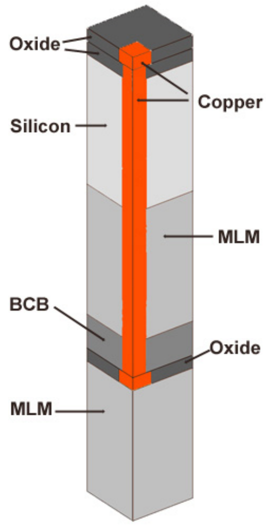

Fig. 2. Schematic of representative simulation cell, constructed using periodic boundary conditions. Horizontal expansion is controlled by the underlying silicon layer. The MLM is treated as a homogenous mixture of 30% Cu and 70% SiO_2 [2, 3]

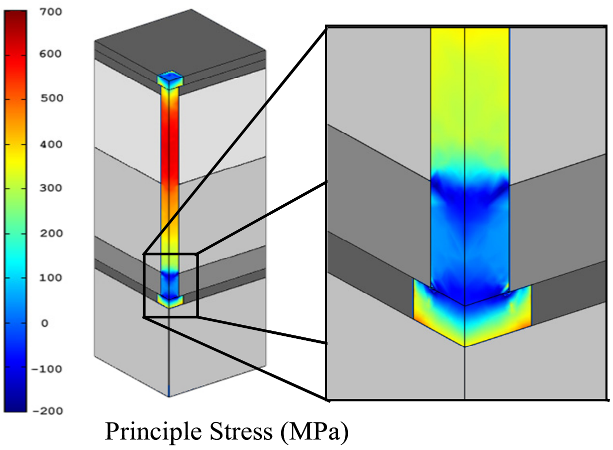

Fig. 3. First principal stresses in a 3D IC via due to a change in temperature from a stress free state at 523 K to 298 K. For clarity, the stress distribution is only shown in the Cu. Stresses are close to or exceed the Cu yield strength; migration and failure are concerns.

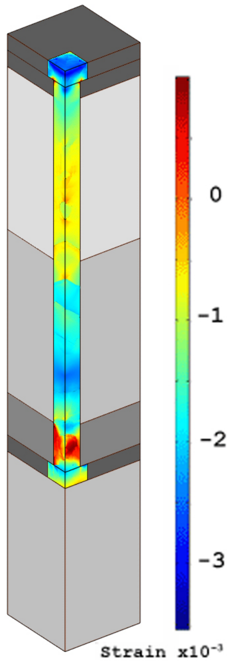

Fig. 4. First principal strains in the Cu 3D IC via due to a change in temperature from 523 K to 298 K, accounting for the internal grain structure using a grain-continuum model. The texture is random and anisotropic materials properties are used. Significant deviations from the continuum results are observed.

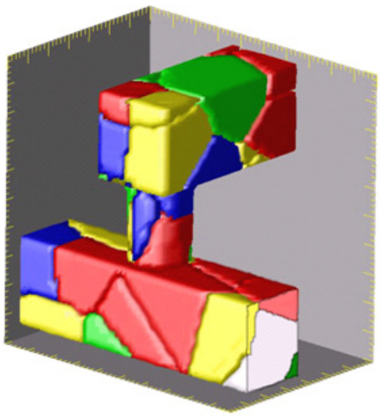

Fig. 5. Example grain structure in a Cu interconnect, developed using PLENTE with random nucleation followed by an isotropic deposition model.