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A 3D Finite Element Parallel Simulator for Studying Fluctuations in Advanced MOSFETs

M. Aldegunde*, A. J. García-Loureiro*, K. Kalna†, and A. Asenov†
*Department of Electronics and Computer Science, University of Santiago de Compostela,
15782 Santiago de Compostela, Spain. E-mail: maldegunde@dec.usc.es
†Device Modelling Group, Department of Electronics & Electrical Engineering,
University of Glasgow, Glasgow G12 8LT, United Kingdom

Polysilicon gates and high-κ dielectrics used in today's MOSFETs are a serious source of intrinsic parameter fluctuations in addition to the random dopants in the channel, source and drain, the line edge, and interface roughness [1]. Limits in doping activation in the polysilicon gate and the doping depletion near the interface result in an unwanted poly depletion effect [2]. The grain structure of the polysilicon is one of the main contributors to the fluctuations, leading to a mismatch in the threshold voltage of sub-100 nm MOSFETs.

Most of the high-κ dielectrics exhibit a thermal instability which leads to local crystallisation of the initially amorphous layer. Regions with different dielectric constant appear which contribute to the intrinsic parameter fluctuations in a device.

In this work, we investigate intrinsic parameter fluctuations introduced by the polysilicon gate and the high-κ dielectric layer using a 3D parallel device simulator. The simulator employs the finite element discretisation in a drift-diffusion (D-D) approximation for the electron transport and runs in parallel employing MPI standard library. We have developed an efficient tetrahedral unstructured mesh generator designed to deal with complicated geometry appearing in sub-100 nm advanced Si MOSFETs in the presence of fluctuations. The mesh is refined close to the boundaries between different regions of the transistor and the zones with the highest variations in the electrostatic potential resulting in a mesh illustrated in Fig. 1. This meshing is also suitable for an accurate description of the polysilicon grain boundaries illustrated in Fig. 2. The simulation domain is partitioned into sub-domains shown in Fig. 3 and assigned to individual processors.

The 3D parallel D-D MOSFET simulator has been calibrated with respect to an *n*-type 67 nm effective gate length Si MOSFET [3]. Fig. 4 compares I_D-V_G characteristics obtained from the 3D D-D parallel simulator with experimental data. It also shows results obtained when the SiO_2 gate dielectric is replaced with a high-κ one with a dielectric constant of 20 (HfO_2), and results when considering an interfacial layer of SiO_2 together with relatively large polycrystalline islands of different dielectric constants in the gate dielectric. Finally, the results obtained assuming a Gaussian distribution of different dielectric constants with a correlation length of 3 nm mimicking fine grains of different orientations in the high-κ gate dielectric layer are presented as well. Fig. 5 shows a semilogarithmic plot of electron density in the 67 nm MOSFET. The effect of intrinsic parameter fluctuations in the polysilicon gate and in the high-κ dielectric layer will be also studied in a template 25 nm gate length bulk MOSFET. As an example, in Fig. 6, we show the electron density right below the semiconductor-insulator interface in the case when the dielectric layer consists of two regions with different dielectric constant separated by a plane $y = 0$.

References

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[3] K. Rim et al., *Strained Si NMOSFETs for high performance CMOS technology*, Symp. VLSI Technol., Dig. Tech. Pap., 59 (2001).

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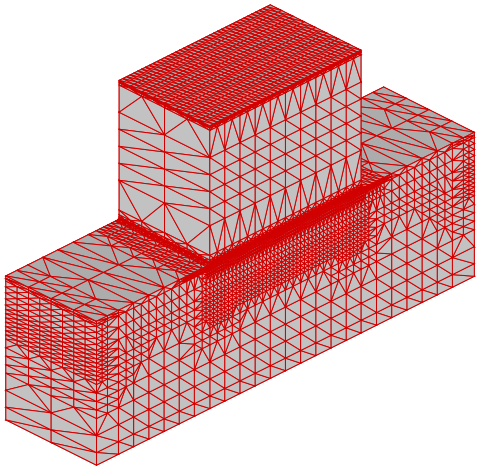

Fig. 1. Finite element mesh for simulation of the 67 nm effective gate length Si MOSFET with a polysilicon gate.

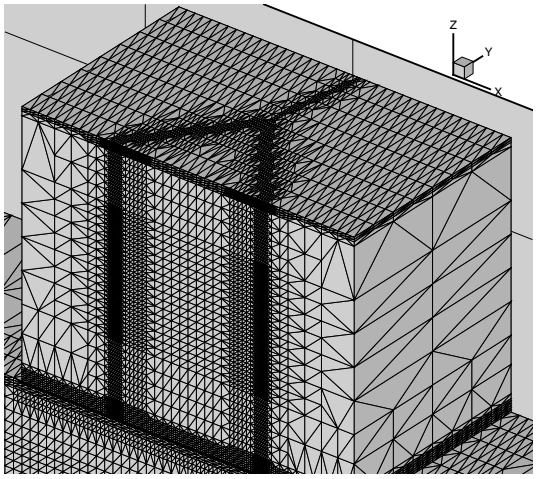

Fig. 2. Detail of a gate meshed for the simulation of three grains in polysilicon.

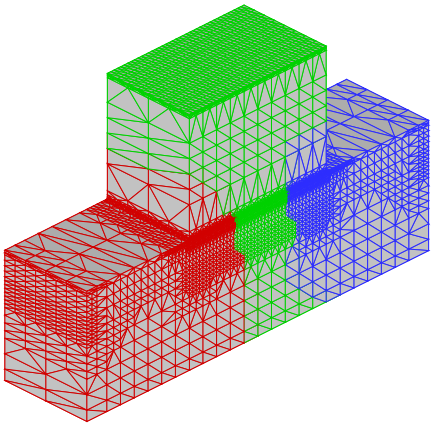

Fig. 3. Partition of the finite element mesh in three subdomains.

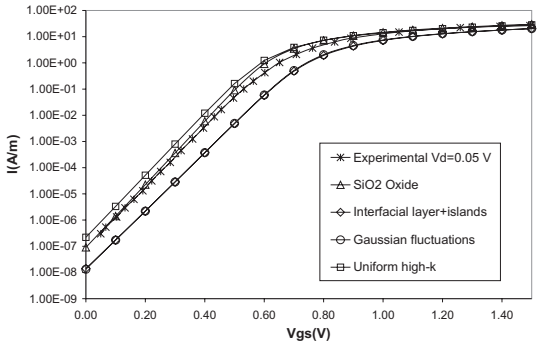

Fig. 4. $I_D - V_G$ characteristics obtained from the 3D D-D parallel simulator compared with experimental data for the 67 nm effective gate length Si MOSFET.

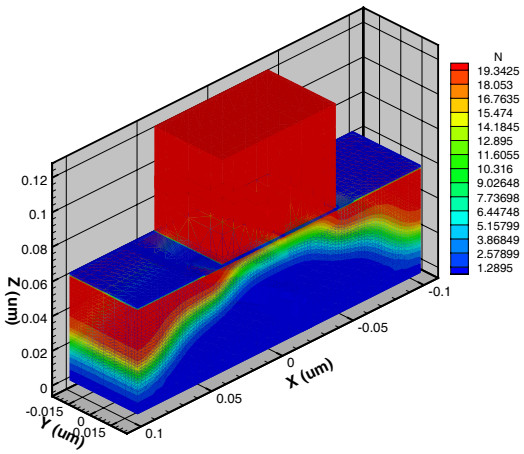

Fig. 5. Electron density on log scale in the 67 nm effective gate length Si MOSFET at $V_G = 0.5V$ and $V_D = 0.05V$.

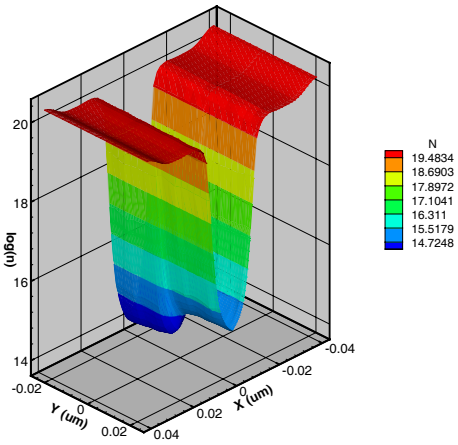

Fig. 6. Electron density at equilibrium beneath a dielectric layer with two different dielectric constants of 7 (Si_3N_4) and 5 in the template 25 nm gate length bulk MOSFET.