Power•Delay Product in COSMOS Logic Circuits

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As CMOS devices explores its fundamental scaling limits, there is a clear consensus that planar MOSFET architecture will be replaced with novel SOI devices incorporating one or more of performance enhancing features such as strain engineering, multiple-gates, heterostructure channels and contacts [1,2]. In accordance with this trend, we have recently purposed a unique CMOS device pair called COSMOS that integrates *n-* and *p*-type MOSFETs both vertically and laterally in an orthogonal layout using strained Si/SiGe on SOI technology [2,3]. Previously, we have shown that COSMOS devices are especially suitable for low-voltage and area-tight designs, due to its inherent reduction in active area and parasitics [4,5]. However, these analyses were based on a simple inverter circuit and did not consider power•delay product, which is the focus of this work.

Fig.1 shows the 3D perspective view of a COSMOS inverter gate. The COSMOS architecture relies for operation on several important structural modifications. For the transport, a thin silicon layer (electron channel) must be grown atop a strained SiGe hole channel. Alternatively, flip-bond on SOI may be used to this end [6-8]. To facilitate threshold tuning, reduce parallel conduction and eliminate need for doping, Ge concentration in the strained channel must be high. In accordance, the gate material may be a mid-gap metal, poly-SiGe alloy or polySi, depending on the choice of Ge concentration. For a layer structure with a 3nm strained-$Si_{0.3}Ge_{0.7}$ hole channel and 2nm Si electron channel under a mid-gap metal gate, 3D TCAD simulations indicate that symmetric MOSFET characteristics (Fig.2) can be obtained using only a single gate. Typically we can achieve a threshold $|V_T|=0.4\pm0.2$ V.

To demonstrate the usefulness of COSMOS for digital circuits, the simulated transient response of a 40nm COSMOS NOT gate to an input pulse is provided in Fig.3. Note that there is no additional manufacturing steps or structures needed for the NOT gate except a *short* metallization layer, hence reducing total RC losses considerably. Clearly, the single gate COSMOS inverter is operational with acceptable noise margins and delay (~100ps).

In the present work, we report the result of 3D simulations to analyze and optimize the temporal response of larger COSMOS circuits such as the NOR gate shown in Fig.4. All our simulations are carried out using ISE TCAD suite [9], which allows accurate 3D meshes and advanced transport models to be incorporated. The transient response of the NOR gate (Fig.5) confirms that output remains low except the '00' input to the gates for a rail-to-rail ($V_{DD}+|V_{SS}|$) voltage of 0.6V. Further simulations at higher voltages (Figs.6&7) indicate that, while the NOR gate is operational, its leakage performance and noise margin deteriorate rapidly above $V_{DD}+|V_{SS}|=0.8V$. At the same time, however, the delay improves rapidly, indicating the importance of optimizing power•delay product in COSMOS circuits.

At the heart of the power versus delay trade-off in COSMOS circuit is the static leakage stemming from the intrinsic formation of 90°-bent *p-i-n* diode between the V_{DD} and V_{SS} contacts. Since the number of such contacts in close proximity increases in logic gates with multiple inputs, large-scale COSMOS circuits can radically benefit from identification of power•delay 'sweet spots' being explored in this work. Furthermore it is possible to reduce the static leakage by i) raising the V_T above 0.3V in the present circuits, for instance by relaxing oxide thickness slightly, which can be tolerated in such ultra-thin channels, ii) adding an extra stop etch beneath the top Si electron channel as opposed to a single etch used in the original COSMOS design [4], and iii) optimizing the device layout by way of shifting the center of the COSMOS cross [10].

We focus on the implementation and comparison of above approaches in choosing suitable power•delay products in large-scale COSMOS circuits. Therefore the present work will assess and explore COSMOS designs in more realistic settings.

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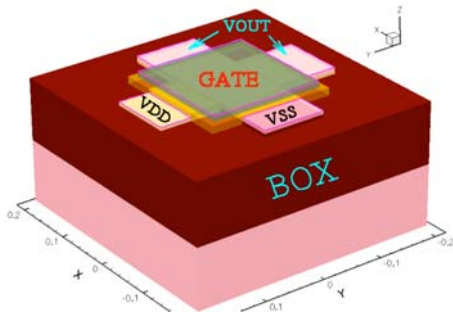[10] A AlAhmadi and S. Kaya, *Sol-State Elec*., submitted

FIGURE 1: FIGURE 1: 3D view of the COSMOS device (L=200nm) and the 3D simulation domain.
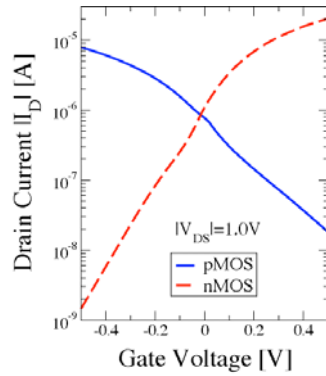

FIGURE 2: Simulated I-V plot in 3D. QM corrections are omitted in this case to save time, e- and h+ mobility are unequal
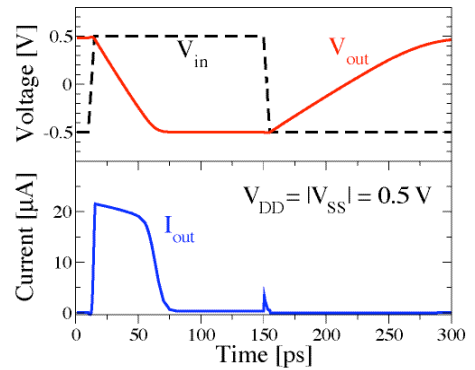

FIGURE 3: Output response of a 40 nm COSMOS inverter to high and low logic inputs of ±0.5V, illustrating logic functionality using a single gate
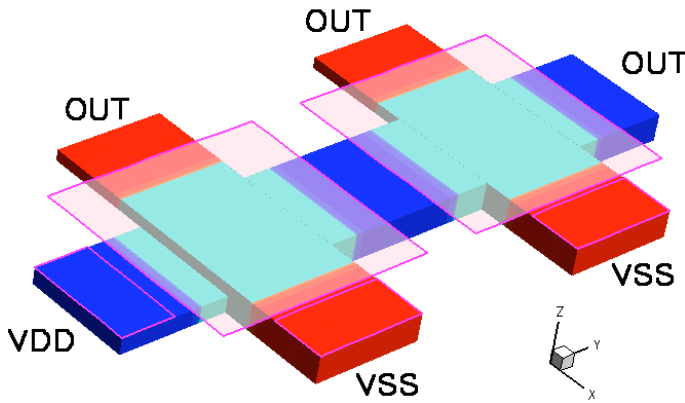

FIGURE 4: The 3D view of a two-input NOR circuit using only two COSMOS gates. All contacts are labeled and gates are shown in semi-transparent fashion to aid the reader. Note that the two nMOSFETs are aligned in parallel while the two p-MOSFETs are in series.
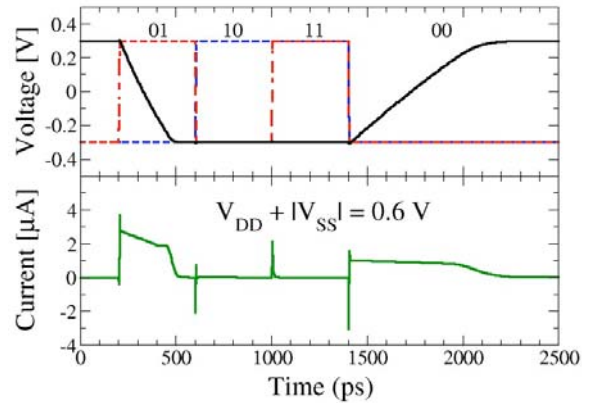

FIGURE 5: The transient response of output voltage (top) and total supply current (bottom) in the COSMOS NOR gate with 40nm gates (see Fig.4). The top figure also includes the input waveforms to the two gates. Only '00' input produces a high output.
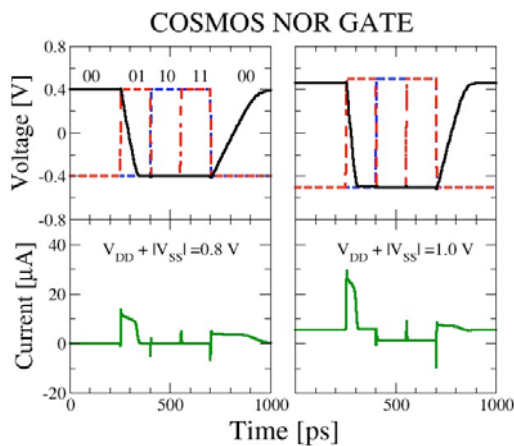

FIGURE 6: Similar to Fig.5 except at higher rail-to-rail voltages. At larger bias conditions the static leakage through the of 90°-bent *p-i-n* diode becomes visible as well as the deterioration of the noise margins.
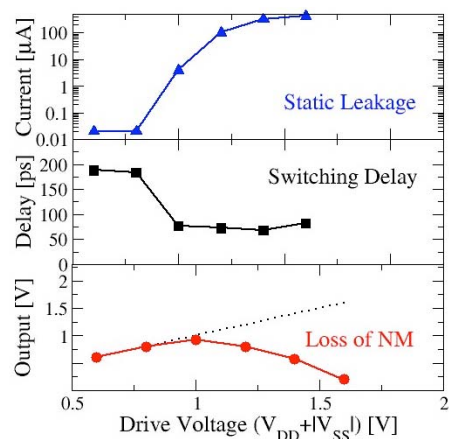

FIGURE 7: Summary of major performance figures for the COSMOS NOR gates driven at different rail-to-rail voltages. Note that optimum power*delay product is likely to be between 0.8 to 1.0V in this circuit.

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