Code for the 3D simulation of nanoscale semiconductor devices, including drift-diffusion and ballistic transport in 1D and 2D subbands, and 3D tunneling

G. Fiori[1], G. Iannaccone[1,2]
[1]Dipartimento di Ingegneria dell'Informazione: Elettronica, Informatica, Telecomunicazioni, Università degli studi di Pisa, Via Caruso, I-56122, Pisa, Italy
[2] IEIIT-CNR, Via Caruso, I-56122, Pisa, Italy. { g.fiori,g.iannaccone}@iet.unipi.it

Device modeling tools capable to address different degrees of quantum confinement and different transport regimes are required to address both MOSFETs at the end of the ITRS Roadmap and alternative device structures. In this work, we present a code based on the self-consistent solution of the *i)* many particle Schrödinger equation based on density functional theory, *ii)* on the nonlinear Poisson equation, and *iii)* on the continuity equation for electrons and holes, in the cases of both drift-diffusion and ballistic transport regimes. In addition, different regions with arbitrary degrees of quantum confinement may be considered, and transport in such regions is consequently computed. If in a given region charge carriers are quantum confined in one direction (2D confinement), transport (ballistic or drift-diffusive) is computed in 2D subbands. Analogously, if charge carriers are confined in two directions (1D confinement), transport is computed in 1D subbands. When transport between two regions occurs via tunneling, the two regions are typically considered electrically insulated, so that the continuity equation is not solved in the self-consistent scheme. Then, once the potential and charge profiles are obtained, as a post processing procedure, tunneling currents are computed using a routine for the computation of scattering matrices in three-dimensional domains. We will show that a series of nanoelectronic devices can be addressed with such a tools, with a computing time often comparable to that of commercial - semiclassical - TCAD packages.

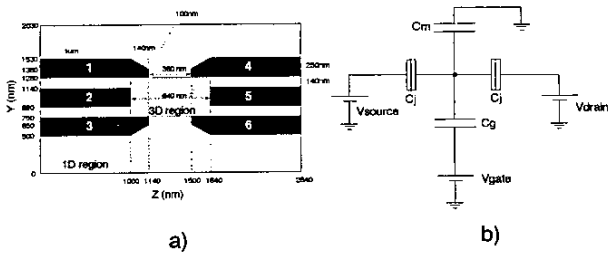
First, we present an example of the simulation of a single electron transistor defined by split gates on a AlGaAs/GaAs heterostructure. In Fig. 1b the gate layout of the considered device is shown. Two different types of confinement have been taken in the same domain: three-dimensional in the central region corresponding to the dot, and one-dimensional in the two-dimensional electron gas (2DEG). The electrochemical potential, computed with Slater's rule, is shown in Fig. 2 as a function of the gate voltage applied to gates 2 and 5.

The drain-to-source conductance as a function of the gate voltage can be easily obtained from the computation of the conductance of each quantum constriction in correspondence of the gate voltage for which the electrochemical potential aligns with the Fermi level.

As a second example, we present the simulation of a silicon nanowire transistor, shown in Fig. 3), with channel length $L = 7$ nm. Here, quantum confinement occurs in the x and z directions. Transport occurs in one-dimensional subbands in the y direction. In Fig. 4 we plot the transfer characteristics obtained by assuming Drift-diffusion transport in the 1D subbands, ballistic transport in the 1D subband, both including or not including source-to-drain tunneling.

In conclusion, our code is a very versatile tool for the investigation of the electrical properties of a broad range of nanoscale semiconductor devices. We gratefully acknowledge support from the EU through the project NANOTCAD and the Network of Excellence SINANO, and from the Fondazione Cassa di Risparmio di Pisa.

A full journal publication of this work will be published in the Journal of Computational Electronics.



a) b)

FIG. 1. a) AlGaAs heterostructure; b) Split gate layout and considered quantum confinement.

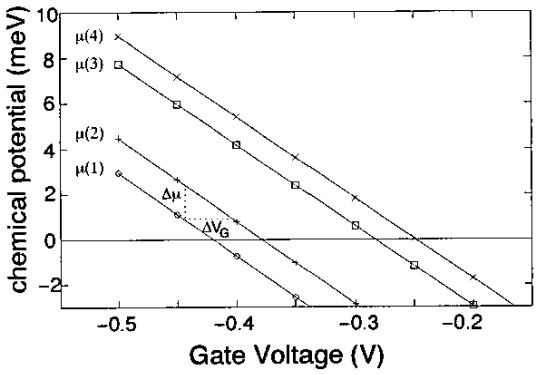


FIG. 2. Computed electrochemical potential as a function of the voltage applied to gates 2 and 5.

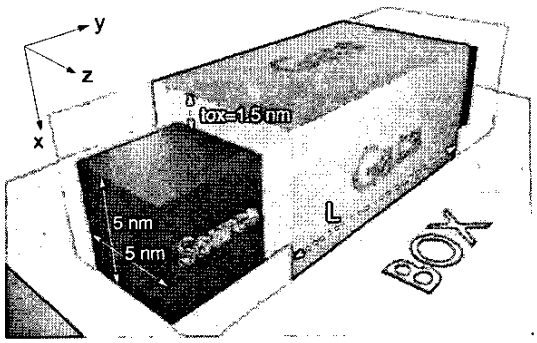


FIG. 3. Structure of the considered silicon nanowire transistor.

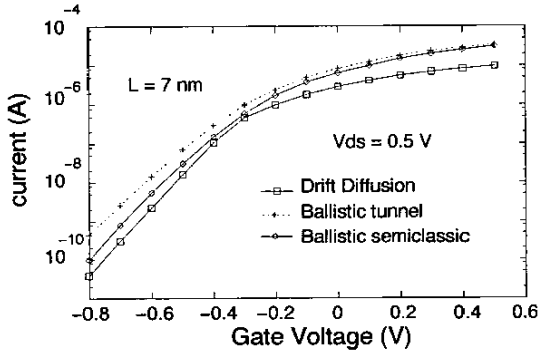


FIG. 4. Transfer characteristics of the SNWT device with channel length equal to 7 nm.

A full journal publication of this work will be published in the Journal of Computational Electronics.