Quantum Potential Approach to Modeling Nano-MOSFETs

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In this work we propose a novel *parameter-free* effective potential scheme for use in conjunction with particle-based simulations. The method is based on perturbation theory around thermodynamic equilibrium and leads to a quantum potential which depends on the energy and wavevector of each individual electron. The quantum potential is derived from the idea that the Wigner equation and the Boltzmann equation with the quantum corrected potential should possess the same steady states. Therefore:

$$W\{\exp(-\beta H[V])\} = \exp\left[-\frac{\beta\hbar^2k^2}{2m^*} - e\beta V^Q(x,k,\beta)\right], \tag{1}$$

where $H[V] = -\frac{\hbar^2}{2m^*}[\nabla_x]^2 + eV$ holds and $W\{\rho\}$ denotes the Wigner transform. In the presence of barriers in a device region, $V = V_H + V_B$ and the resulting quantum potential $V^Q(x,p)$ is then given by [1]:

$$V^Q(x,k) = \frac{1}{(2\pi)^3}\int\frac{2m^*}{\beta\hbar^2k\cdot\xi}\sinh\left(\frac{\beta\hbar^2k\cdot\xi}{2m^*}\right)\exp\left(-\frac{\beta\hbar^2}{8m^*}|\xi|^2\right)\int V(y)e^{i\xi\cdot(x-y)}dyd\xi \tag{2}$$

Note that the barrier potential $V_B(x)$, is one-dimensional and independent of time and needs to be computed only once in the initialization stage of the simulation. The effect of the barrier potential/field on the operation of a 25 nm MOSFET has already been investigated and published elsewhere [2]. On the other hand, the Hartree potential is two-dimensional and time-dependent as it describes the evolution of charge from a quasi-equilibrium to a non-equilibrium state. Since the evaluation of the effective Hartree potential as given by Eq. (2) is very time consuming and CPU intensive, approximate solution methods have been pursued to resolve this term within a certain level of error tolerance.

This approach, with both the barrier and the Hartree potential corrections, has been applied to modeling transport in a nano-scale MOSFET with gate length of 25 nm. The oxide thickness is 1.2 nm. Fig. 1 shows the charge set-back from the interface proper that degrades the oxide capacitance and, therefore, the MOSFET transconductance. The impact of the Hartree correction is found to be lesser than that of the barrier potential, which is depicted in the device transfer and output characteristics (Figs. 2 and 3 respectively). One can also see that quantization gives rise to an on-state current reduction of about 20% and an increase in the threshold voltage. The simulation results have been compared to those obtained by using the approach due to Ferry and co-workers [3].

[1] C. Ringhofer, C. Gardner, and D. Vasileska, *Intl. J. High Speed Electr.*, Vol.13, pp. 771, 2003.
[2] S. Ahmed, C. Ringhofer, and D. Vasileska, *J. Comp. Electr.*, Vol. 2, pp. 113–117, 2003.
[3] D. K. Ferry, R. Akis, and D. Vasileska, *IEDM Tech. Dig. (IEEE Press, New York)*, pp. 287, 2000.

A full journal publication of this work will be published in the Journal of Computational Electronics.

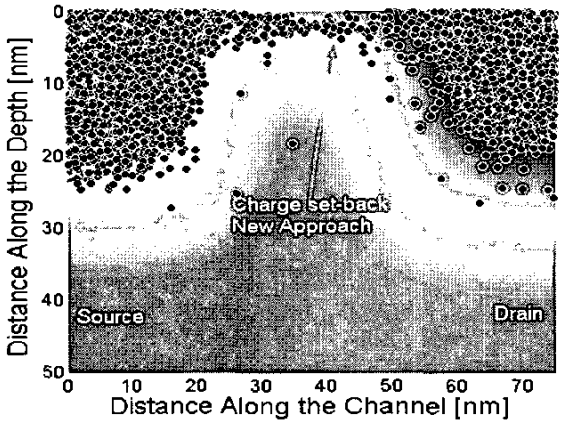

Fig. 1. Distribution of the electrons for $V_G = 1.2$ V and $V_D = 1$V.

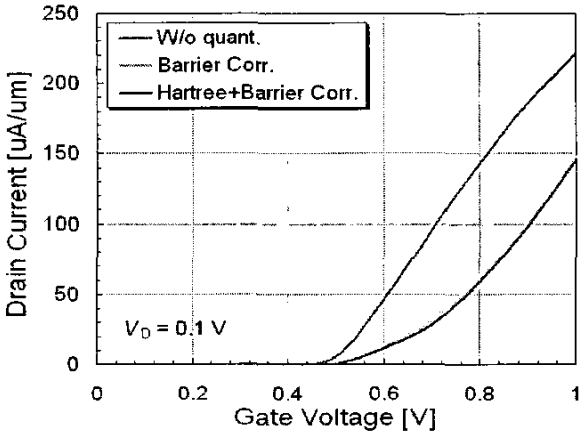

Fig. 2. Device transfer characteristics for $V_D = 0.1$V.

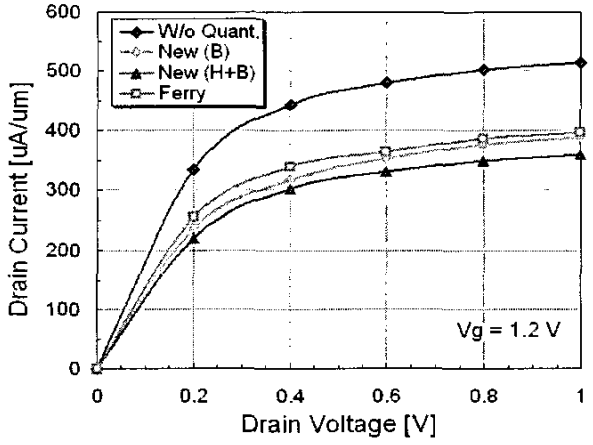

Fig. 3. Device output characteristics for $V_G = 1.2$V (H: Hartree/B: Barrier).

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