A Microscopic Quantum Simulation of Si/SiO_2 Interface Roughness Scattering in Silicon Nanowire Transistors

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The Silicon Nanowire Transistor (SNWT) has attracted broad attention as a promising device structure for future integrated circuits [1-4]. As a result, the exploration of carrier transport and the modeling of various scattering mechanisms in Si nanowires become increasingly important. In this work, we perform a microscopic, quantum-mechanical simulation of Si/SiO_2 interface roughness scattering (so called "surface roughness scattering (SRS)") [5-10] in SNWTs.

The effects of Si/SiO_2 interface roughness on carrier transport are as follows: 1) the roughness introduces electrostatic potential variations inside the Si body, which behave as a scattering potential for carriers, 2) due to the Si/SiO_2 conduction band-edge discontinuity, the roughness causes a fluctuating electron subband energy and wavefunction shape, which lowers the transmission from the source to the drain (so called "wavefunction deformation scattering" [6-8]). In SNWTs with very small diameters (e.g., <5nm), both effects become substantially important and a direct treatment of SRS in a quantum mechanical framework is necessary.

Figure 1 illustrates the simulated structure in this work. The simulation region is discretized with a 3D finite element mesh [11]; each element is a triangular prism with a comparable size to the roughness at the (100) Si/SiO_2 interfaces [12-13]. A 2D random distribution is generated across the Si/SiO_2 interfaces according to the relevant auto-covariance function [12], and based on this random distribution, the (material) types of the elements (prisms) at the Si/SiO_2 interfaces may be changed from Si to SiO_2 or reversely, to mimic the roughened interfaces. The roughened SNWT is then simulated by the non-equilibrium Green's function approach [14]. By using the coupled mode space approach [11], the wavefunction deformation due to the Si/SiO_2 interface roughness is adequately treated. To emphasize the role of SRS on electron transport, we do not include any other scattering mechanisms, so electron transport is coherent inside the device. The simulation results for the roughened device are then compared with those for a device structure with the same geometrical parameters but smooth Si/SiO_2 interfaces, which is treated as the *ballistic* device.

Figures 2 and 3 illustrate the effects of SRS on both the internal parameters (e.g., subbands, transmission) and current-voltage characteristics of the simulated SNWT. It is found that 1) SRS significantly deforms the electron subbands in the SNWT, 2) SRS blocks low-energy injections from the source into the channel, so it reduces the density-of-states (DOS) at low energy and consequently raises the threshold voltage of the device, 3) due to the DOS degradation caused by SRS, the roughened SNWT displays lower subband levels at the top of the barrier under ON-state conditions, which somehow compensates the reduction of transmission due to SRS at the ON-state, and 4) the transmission reduction caused by SRS becomes quite significant when more than one subbands become conductive (this is consistent with the observation that SRS is very important in planar MOSFETs, where a large number of transverse modes are conductive). In brief, this work provides an opportunity to understand the physics of SRS in SNWTs, which can be substantially different from that in planar MOSFETs.

A full journal publication of this work will be published in the Journal of Computational Electronics.

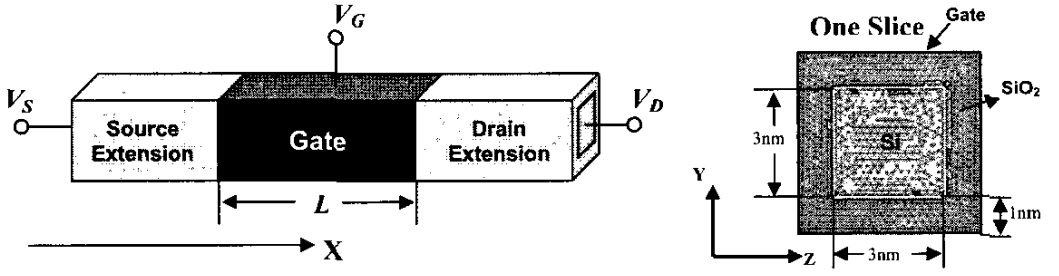

Fig. 1 The schematic diagram of the simulated gate-all-round SNWT with a rectangular cross-section ($L=10nm$). The X, Y, and Z coordinates are in the (100), (010) and (001) crystal orientations, respectively. The right figure shows a slice of the SNWT with a roughened Si/SiO_2 interface (please note that the pattern of the roughness varies from slice to slice).

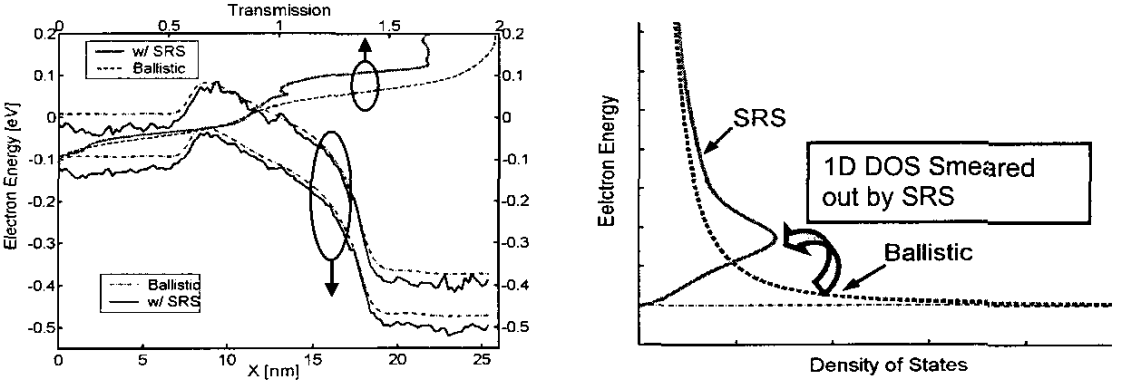

Fig. 2 The electron subband profile and transmission coefficient for the simulated SNWT with and without (ballistic) SRS (left). The device is at the ON-state (i.e., $V_{GS}=V_{DS}=0.4V$), so the source and drain Fermi levels are located at $0eV$ and $-0.4eV$, respectively. The right plot illustrates the DOS reduction at low energy caused by SRS.

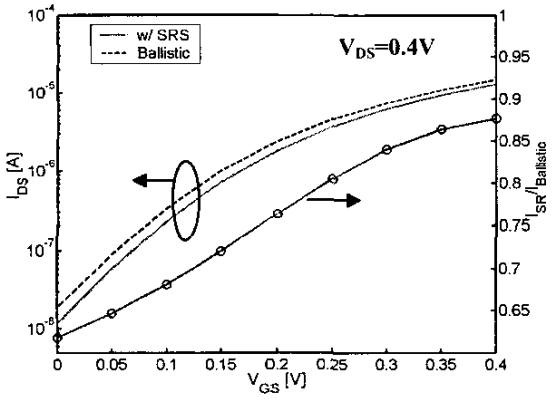

Fig. 3 The *I-V* characteristics (left) of the simulated SNWT and the ratio (right) of the current for the roughened structure, I_{SR}, to the ballistic current, $I_{Ballistic}$.

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