Scattering from body thickness fluctuations in Double Gate MOSFETs. An *ab initio* Monte Carlo simulation study.

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The scaling of the conventional MOSFETs is running out of steam due to the extremely high doping and thin gate oxides required to suppress short channel effects, but these requirements degrade mobility and drive current and introducing unacceptable junction and gate leakage. It is expected that Ultra Thin Body (UTB) SOI or Double Gate (DG) transistors will replace the conventional MOSFETs somewhere at or beyond the 45 nm Technology node [1,2]. A major unresolved problem associated with the introduction of UTB devices is an acute mobility degradation observed experimentally for body thicknesses below 5 nm, which are required for the scaling of the DG transistors below 10 nm channel lengths. Many factors including surface roughness, surface optical phonon and Coulomb scattering contribute to the mobility degradation in competition with volume inversion induced mobility enhancement [3,4], but cannot explain the full magnitude of this effect. Only recently it has been suggested that the variation in the subband energy levels along the channel introduced by the body thickness variation, as illustrated in Fig. 1, and scattering from the corresponding quantum potential barriers in the constrained regions play a major role in the body thickness induced mobility degradation [4,5]. For channel lengths of 10 nm and below each double gate transistor will have a unique body thickness pattern introduced by surface roughness at the top and bottom interface. This inevitably introduces 'intrinsic' variations in the transport and in the drive current from device to device which will severely affect their integration in modern and future chips, containing on the order of a billion transistors.

In this paper we present an *ab initio* approach for including body thickness variation effects in 3D Monte Carlo simulation studies through the real space trajectories of Monte Carlo particles moving and scattering in the presence of a quantum potential obtained from the solution of the density gradient equation [6]. This approach is used to study the mobility degradation associated with body thickness variation in large self-averaging devices and the transport and performance variation in small devices introduced by the unique body thickness pattern in each one of them.

Simulations are carried out at low-drain voltage in a frozen field approximation. The double gate transistors are simulated first using a 3D drift diffusion simulator with density gradient quantum corrections. Then the obtained electron density is used to initiate the particles in the Monte Carlo simulation module, which includes all major scattering mechanisms relevant for silicon except for surface roughness scattering, this being included *ab inito*. The simulated particles are moved and scattered following the standard Monte Carlo procedure but using the quantum potential to calculate the effective driving force during the free flights. The quantum potential, which closely follows the ground state contains information about the rough interfaces and the potential landscape which will scatter the carriers within the constrained regions of the channel. Figs. 2 and 3 illustrate the results from 3D drift diffusion simulations of a 10×10 nm UTB DG, which is the starting point for the Monte Carlo simulation. Quantum confinement keeps the carriers in the middle of the channel. The variation in the carrier concentration and the potential distribution associated with the random top and bottom interfaces and the corresponding body thickness variations are clearly visible. In the middle of the channel, however the classical potential, illustrated in Figs. 4a and 5 is relatively smooth and will not introduce significant scattering when used to calculate the driving force. However, the quantum potential in Figs. 4b and 5 exhibits significant potential variations, which results in additional scattering. Fig. 6 illustrates preliminary results for the body thickness dependence of the mobility when both smooth top and bottom interfaces are assumed in a large device, showing a small variation with thickness as expected. Results for variations in mobility and corresponding variations from device to device, due to body thickness fluctuations in the UTB are in process of simulation now and will be presented at the conference.

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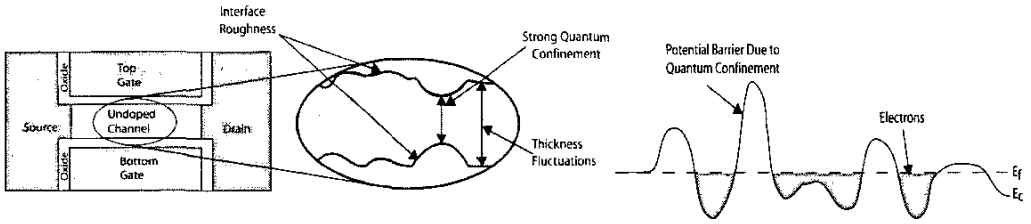
A full journal publication of this work will be published in the Journal of Computational Electronics.



(a) (b)

Figure 1: (a) Variations in body thickness reuslting from interface roughness between the silicon and the oxide layers, and (b) the potential barriers associated with these additional constaints.

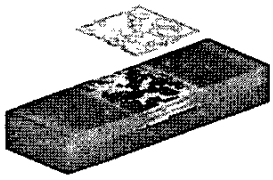


Figure 2: Schematic of Double Gate structure with top gate removed to show carrier concentration at the top interface. Shows the peak concentration of carriers to be through the centre of the channel.

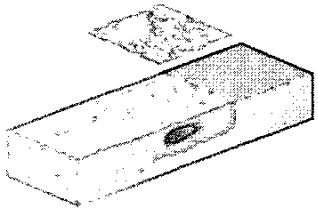
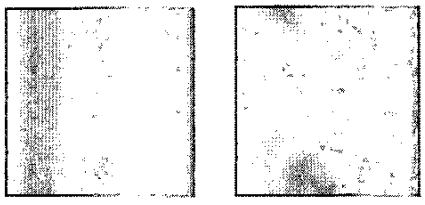


Figure 3: Electrostatic potential in the Double Gate device. The top gate is removed here to show the top interface displaying fluctuations in the potential due to variations in the oxide thickness.



(a) (b)

Figure 4: (a) Classical Potential Plane. Taken as a slice through the centre of the channel. (b) Quantum Potential Plane, taken through the centre of the channel, showing fluctuations not present in the classical potential.

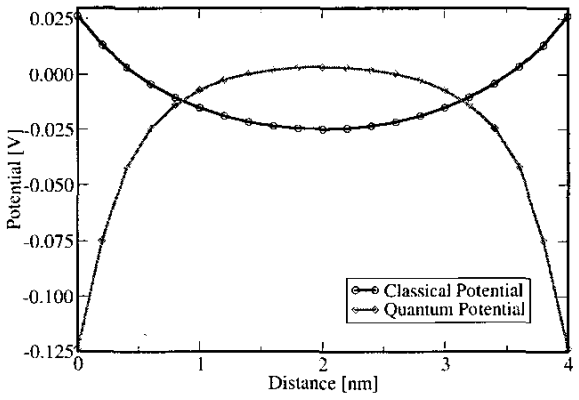


Figure 5: Vertical Potential in Double Gate MOSFET, without interface roughness, running from top interface to bottom.

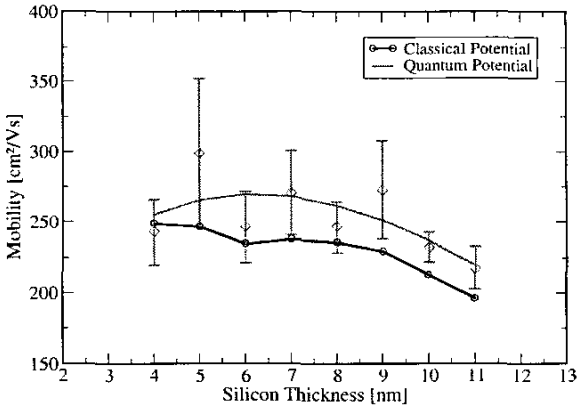


Figure 6: Mobility in the channel, for simulations of smooth devices done with both the classical and quantum potentials.