**Electrostatics of 3D Carbon Nanotube Field-Effect Transistors**

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The electrostatics of a three-dimensional CNFET structure are studied. The paper is an extension to 3D structures, of previous work done for 2D structures. Previous work has shown that one-dimensional channels experience long range doping by the gate and contact electrodes and are very sensitive to the electrostatic environment. We examine how the three-dimensional environment affects the charge transfer from the metal contacts into a 30nm short intrinsic, semiconducting CNT, along the length of the tube under equilibrium conditions.

The charge density in the device is determined by self-consistent calculation of the Poisson equation with equilibrium carrier statistics of nanotubes. The method of moments is used to solve the Poisson equation. Two different experimental structures are examined. Starting from the bottom gate device shown in Figure 1a, the effect of the gate oxide thickness, contact thickness and width, and Schottky barrier height between the contact and the channel are investigated. We examine how these parameters affect the conduction band profiles and the charge in the middle of the channel for various gate biases. The top gate device shown in Figure 1b is then simulated using a high dielectric constant material for the top region of the device. This type of device is one of the most recent experimental structures demonstrated. The effect of the contact thickness, width and top gate oxide thickness is also examined for this type of device.

It is found that both devices are very sensitive to the geometric variations of the electrostatic environment. Variation of the gate oxide thickness has a huge effect on the channel along it's entire length. The devices are expected to perform better for smaller oxide thicknesses. There is smaller but significant sensitivity to the size of the contact, primarily to the part of the contact that is connected to the rest of the device through a higher dielectric constant material, rather than the region that resides in the lower dielectric constant material. The larger the dielectric constant of the material in the region between the contact and the channel, the larger the electric field penetration in the channel. Most of the contact effect, however, comes from the region that is near the channel. Therefore, increasing the contact thickness does not affect the channel directly. Simulations of bottom gate devices with different contact thicknesses showed minimal differences in the charge induced in the channel. Larger contacts affect the channel indirectly, by screening the effect of the gate, for both bottom and top gate devices. This reduces the ability of the gate to electrostatically control the channel. The effect of the Schottky barrier for electrons is also examined, and it is found that it causes a shift in the threshold voltage of the device and in the subthreshold swing. A low barrier results in a locally effective n-type "doping" of the nanotube by the contacts. When the gate is far away from the channel, this effect can penetrate in the entire channel.

The top gate device indicates better characteristics than the bottom gate device, with better subthreshold swing and higher $Q_{on}/Q_{off}$ ratio. The ideal coaxial device examined in previous work, has however better performance than both bottom and top gate devices. A cylindrical gate surrounding the channel provides better electrostatic control. The large contact parasitics of the short channel planar structures make it hard to map the two geometries just by mapping the gate insulator capacitance without taking into account the contacts.

A full journal publication of this work will be published in the Journal of Computational Electronics.

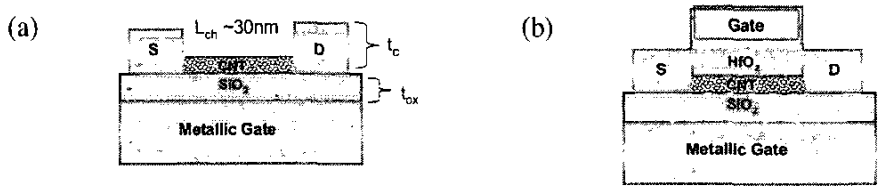


Figure 1: (a) Experimental structure for the bottom gate planar transistor. (b) The top gate device with high dielectric constant material in the top region.

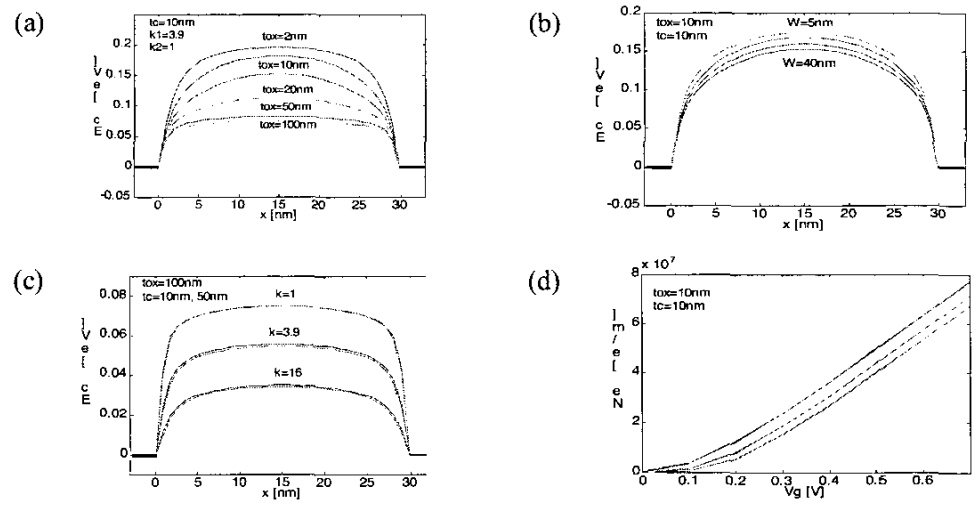


Figure 2: The conduction band profiles for the bottom gate structure for geometric variations, at $V_g$=0V. (a) Variation of the gate oxide thickness. (b) Variation of the contact width (W=5, 10, 22, 40nm). (c) Variation of the top region dielectric material and contact thickness $t_c$ ($t_c$=10nm (blue), $t_c$=50nm (red)). (d) Electron density in the middle of the channel vs. $V_g$ for different Schottky barriers for electrons ($\Phi_{Bn}$=0eV (blue), 0.13eV (green), 0.21eV (red)).

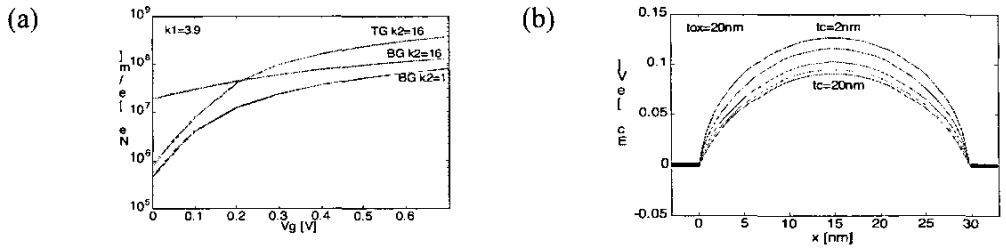


Figure 3: (a) Electron density in the middle of the channel vs. $V_g$ for the bottom gate device with air in the top region, bottom gate device with high dielectric constant material in the top region and top gate device. (b) The effect of the contact thickness for the top gate device on the conduction band profile ($t_c$=2,5,10,15,20nm). The top gate oxide thickness is 20nm.

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