RF Performance of Strained SiGe pMOSFETs: Linearity and Gain

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To continue CMOS scaling in sub-50nm range during the next decade, the use of SOI substrates and strained-Si/SiGe channel layers will be an attractive option [1]. Both approaches can dramatically improve the high frequency performance of MOSFETs due to reduced substrate leakage in the former and enhanced channel mobility and velocity overshoot effects in the latter [2]. A combination of these two approaches is also a possible structure currently investigated, where promising results are already demonstrated experimentally [3]. However, RF performance analysis of this device structure has not received extensive research efforts. In this work, we investigate RF performance of strained-SiGe pMOSFET because of its easy integration into planar architecture than strained-Si nMOSFET. RF figure of merits considered include linearity, intrinsic gain and g_m/I_d. To optimize RF performance, variations of SOI thickness (t_{si}) and Ge concentration in the channel are investigated. Furthermore, since graded channel (GC) MOSFET has been proposed as a candidate of RF application [4], a graded strained-SiGe channel pMOSFET is studied comparatively for RF analysis.

The strained-SiGe pMOSFET structure studied in this work is shown in Fig.1 with a 5nm strained SiGe channel layer. We use 2D device simulator DESSIS to obtain terminal characteristics of our devices [5]. In the simulation, quantum mechanical effects are taken into account using density-gradient corrections. Hydrodynamic transport model is included also to incorporate non-stationary transport in our simulations. Fig.2 shows the equilibrium band diagram of the strained-SiGe channel pMOSFET. For RF figure of merits, g_m/I_d is calculated from DC simulations, linearity (P_{IP3}) is calculated from g_m derivatives using high-order polynomial fits [6], intrinsic gain (g_m/g_d) is extracted from AC simulations. All of the simulations are conducted at the same operation condition (I_{DS}=200μA/μm) to allow fair comparisons.

We first compare the RF performance of ordinary strained-SiGe pMOS with GC strained-SiGe pMOS at different Ge concentrations. The former has an unintentional doping density of 10^{15} cm^{-2} for the whole channel while the latter has a high doping density 10^{17} cm^{-2} in the left half of the channel. . We observe in Fig.3 that, as the Ge concentration increases in the channel, the g_m/g_d improves consistently by as much as 14 (~23dB) in strained-SiGe pMOS, which benefits from an increase in g_m and a decrease in g_d. GC structure has only a small (~5dB) positive impact on g_m/g_d. Fig.5 shows that, by increasing Ge concentration in the channel, the g_m/I_d improves sharply by ~$15V^{-1}$ and the linearity (P_{IP3}) decrease slightly (~2dBm) for undoped SiGe pMOS. The non-uniform channel doping has a slightly negative impact on g_m/I_d and a slightly positive impact on linearity. We also investigate the influence of SOI thickness on RF performance of both undoped and GC devices. From Fig.4, we observe that g_m/g_d increases for both $Si_{0.3}Ge_{0.7}$ and $Si_{0.7}Ge_{0.3}$ pMOS as t_{si} scales down, with a larger (~30dB) improvement for the former case than for the latter case (~23dB). Fig.6 shows that as t_{si} scales down, g_m/I_d increases slightly about $1.5V^{-1}$ for undoped $Si_{0.7}Ge_{0.3}$ pMOS while it has optimal value between 5nm to10nm for $Si_{0.3}Ge_{0.7}$ case. The linearity figures of the same devices do not have a strong dependence on t_{si}.

An understanding of interplay between device parameters as well as incorporation of more elaborate physical models is essential for the use SiGe technology in RF applications. Therefore we investigate how the SiGe pMOSFET layer structure, gate geometry, and doping profiles result in several trade-offs in RF device design, and how TCAD tools may be deployed to search for optimum gain and linearity conditions in a given application.

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[4] B. Cheng *et al.*, *IEEE Int. SOI Conference*, p.113, 1998.
[5] ISE System Inc., TCAD suite, www.ise.com
[6] W Ma, S Kaya and A Asenov, *Proc. of EDMO*, p.255, 2003.

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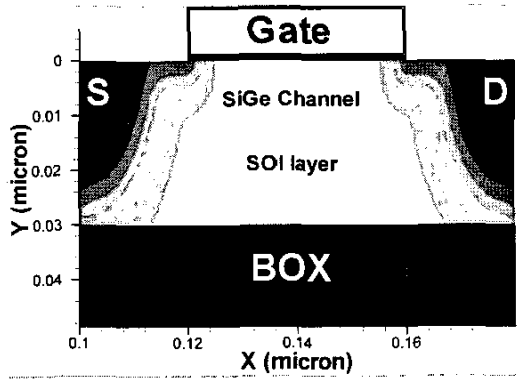

FIGURE 1: Strained-SiGe p-MOSFET structure with L_{eff}=100 nm. Mesh lines for the channel and contacts are indicative of fast varying potentials in these layers.

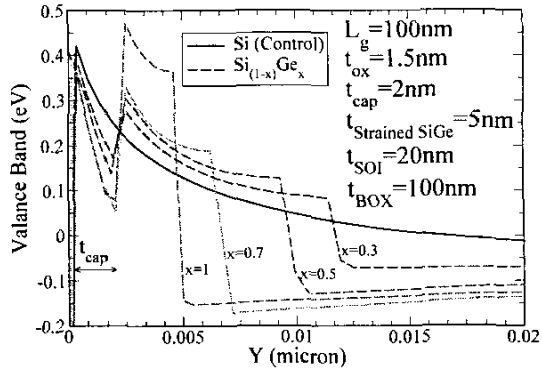

FIGURE 2: Equilibrium band diagram for the structure considered in this work. Note that only the classical potentials are plotted in the band diagram.

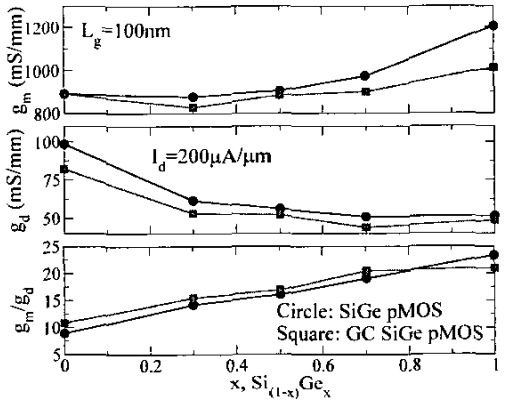

FIGURE 3: Comparison of ordinary strained-SiGe pMOS with GC strained-SiGe pMOS for g_m, g_d and g_m/g_d at different Germanium concentration.

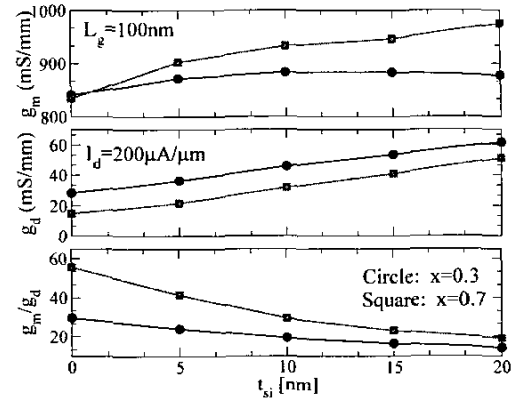

FIGURE 4: Impact of SOI body thickness (t_{si}) on g_m, g_d and g_m/g_d at of strained-$Si_{0.7}Ge_{0.3}$ pMOS and strained-$Si_{0.3}Ge_{0.7}$ pMOS.

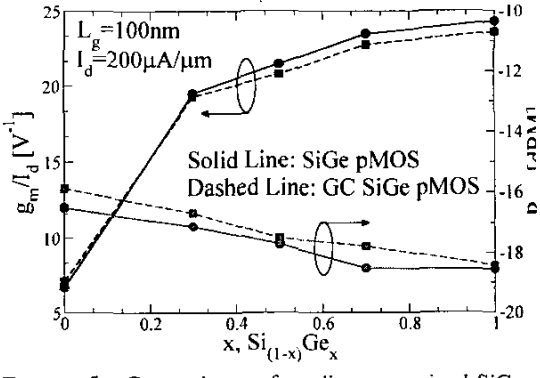

FIGURE 5: Comparison of ordinary strained-SiGe pMOS with GC strained-SiGe pMOS for g_m/I_d and P_{IP3} at different Germanium concentration.

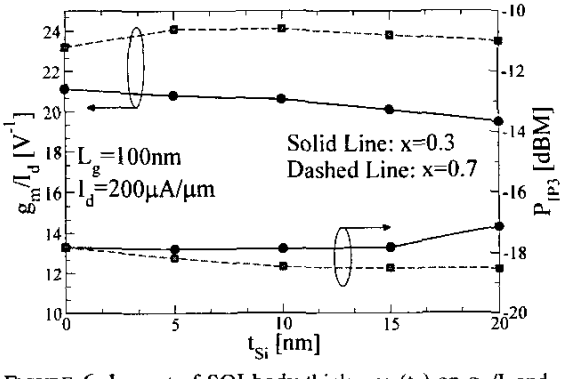

FIGURE 6: Impact of SOI body thickness (t_{si}) on g_m/I_d and linearity (P_{IP3}) of strained-$Si_{0.7}Ge_{0.3}$ pMOS and strained-$Si_{0.3}Ge_{0.7}$ pMOS.

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