Silicon-Germanium Structure in Surrounding-Gate Strained Silicon Nanowire FETs

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Strained silicon devices have been widely studied [1-2]. They possess better driving capacity than that of silicon-based devices. Double-gate strained silicon field effect transistors (FET) have recently been proposed and found better transport characteristics than single gate strained devices [1-4]. For example, double-gate strained silicon FETs not only have relatively high mobility, high transconductance, and ideal subthreshold swing but also suppress short-channel effects (SCEs) [1-2]. Due to superior channel controllability, excellent performance of surrounding-gate FET has also been studied to further reduce SCEs [3-4]; however, these structures have not been well investigated for strained silicon devices.

In this work, , shown in Fig. 1, strained silicon surrounding-gate nanowire FETs are numerically explored and optimized with respect to various physical parameters. In our simulation the region of silicon-germanium Si_xGe_{1-x}, where $x = 0.8$ is simply fixed, channel and source/drain doping is 10^{18} and $5x10^{19}cm^{-3}$, respectively, and mid-gap gate material is TiN. A three-dimensional (3D) quantum correction transport model, density-gradient drift-diffusion model, is applied in the simulation of strained silicon surrounding-gate FETs [4]. It is known that the formulation of mobility is an important factor for strained silicon; however, to focus on the structure optimization of thickness of silicon-germanium, Kaiblinger-Grujin's mobility [5] is implemented in our nanodevice simulator. By fixing other parameters, our preliminary result shows that the thickness of silicon-germanium layer plays an important factor in transport characteristics. Unlike the results obtained from double- and single-gate FETs [1-2], the on/off current ratio and the threshold voltage do not significantly affected by the thickness of silicon-germanium layer. In other words, surrounding-gate strained silicon FET obtains a higher driving current without significantly changes in threshold voltage and on/off current ratio. These characteristics are attractive in nanodevice era. Figure 1 shows a cross-section view of the optimized FET structure. The simulated structure is a silicon-germanium nanowire covered by a silicon layer. The radius of surrounding-gate nanowire FET is 5 nm and the gate oxide thickness is 1 nm. Among several physical quantities, we take here the I_D-V_D characteristics as a benchmark in the optimization of strained silicon FET structure with respect to the radius of silicon-germanium (R_{SiGe}). Figures 2(a) and 2(b) show potential distributions for both pure silicon and strained silicon FETs, where the radius of silicon-germanium nanowire is 4 nm which is covered by 1 nm silicon film. We find that the distributions are almost the same for both samples. Cutting from the center of nanowire, cross-section plot of potential distribution, shown in Fig. 3(a), indicates that there is only slightly difference between them. Fig. 3(b) confirms that the difference of the threshold voltage and the on/off current ratio among different testing conditions are small. Strained silicon nanowire FET structures do not change the transfer characteristics of surrounding-gate devices even the silicon-germanium is naturally with a smaller band gap than that of silicon. This consequence is caused from the fact that the surrounding-gate nanowire FET has excellent channel controllability. Therefore, suppression of leakage current is enhanced from the band gap narrowing. Based on our calculation, it is found that one of the most attractive characteristics for the surrounding-gate strained silicon nanowire FET is the improvement of driving current. As shown in Fig. 4, strained silicon nanowire FET structures have a higher drain current than that of the pure silicon structure (i.e., $R_{SiGe} = 0$ nm). Furthermore, it could be also found that the larger silicon-germanium radius ($R_{SiGe} = 4$ nm) implies the higher drain current. It is due to a higher stress caused from the thinner silicon film.

In this paper, we have investigated the thickness effect of silicon-germanium for surrounding-gate strained silicon nanowire FETs by our developed 3D nanodevice simulator. R_{SiGe} influences the driving current characteristic of surrounding-gate strained silicon nanowire FETs. A large R_{SiGe} increases the driving current and does almost not change the transfer

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characteristics. We are currently working on more advanced structure and device characteristic optimization with respect to various physical parameter including component effect of Si_xGe_{1-x}.

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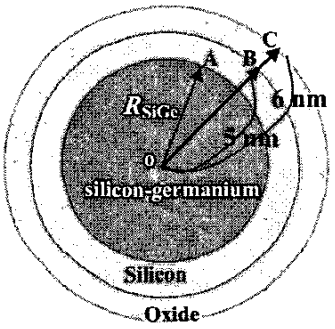

Figure 1. A cross-section view of the surrounding - gate strained Si nanowire FET. The oxide thickness (BC) is 1 nm and the layer radius (oB) of silicon film and silicon-germanium is 5 nm.

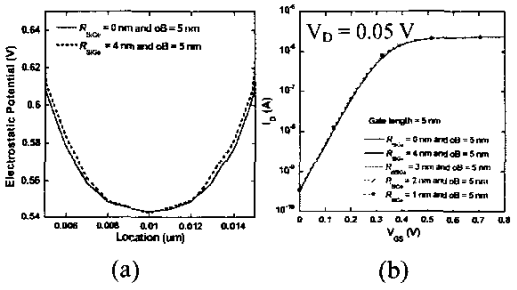

Figure 3. (a) A cross-section view of the electrostatic potentials and (b) the transfer IV characteristics of the surrounding-gate pure and strained silicon nanowire FETs.

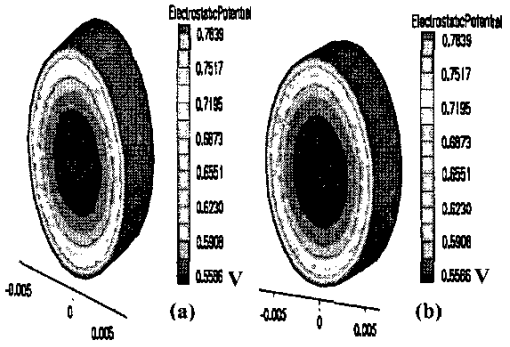

Figure 2. The computed electrostatic potential of the surrounding-gate (a) pure and (b) strained Si nanowire FET, where V_{GS} = 0.5 V and V_D = 0.05 V.

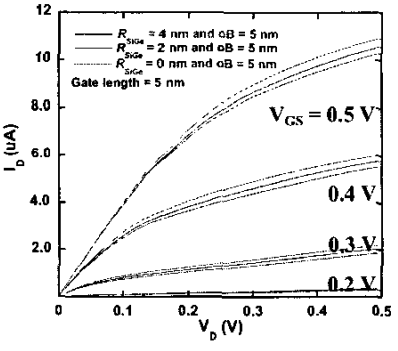

Figure 4. The driving current IV characteristics of both surrounding-gate pure and strained silicon nanowire FETs.