Intrinsic Parameter Fluctuations in Conventional MOSFETs at the Scaling Limit: A Statistical Study

F. Adamu-Lema*, G. Roy, A. R. Brown, A. Asenov, and S. Roy
Device Modelling Group, Dept. E&EE, University of Glasgow, Glasgow, G12 8LT, UK
*Email: fikru@elec.gla.ac.uk, Tel: +44 141 330 4792, Fax: +44 141 330 4907

Conventional MOSFETs with 40 nm channel lengths at the 90 nm technology node (TN) have already been successfully developed and integrated into commercial products [1]. Promising 25 nm gate length (L_G) conventional devices, required for the 65 nm TN, have also been reported [2], and are expected to deliver the performance required by the ITRS[3] using optimized processes. There is, however, growing evidence that beyond the 45 nm TN it will become necessary to replace conventional MOSFETs with novel architectures, complimented by technology boosters such as SOI and strained silicon. Conventional MOSFETs with L_G below 25 nm require excessive channel doping to minimize short channel effects. This doping adversely affects carrier mobility and therefore drive current, and increases junction leakage through band to band tunnelling [4]. In addition, intrinsic parameter fluctuations, resulting from the granularity of matter in such small MOSFETS, have emerged as a major scaling limitation for conventional devices. For example recent studies show that random doping fluctuations have already adversely affected the yield of SRAM cells at the 90 nm TN. To ensure reliable operation in the presence of these fluctuations the *cell ratio* must be increased from its nominal value [5]. This leads to an increased cell area and thus compromises SRAM scaling, and hence the scaling of the majority of silicon based digital systems.

The intrinsic parameter fluctuations induced by random dopants into the characteristics of ultra-small CMOS devices have previously been studied using 3D numerical simulation of predominantly idealised devices [6]. In this paper we present a simulation study of intrinsic parameter fluctuations in carefully scaled realistic MOSFET devices at the next three technology nodes. The scaled devices are based on a real 35 nm transistor reported by Toshiba [7] and depicted in Figure 1. It has been used to thoroughly calibrate our atomistic device simulator [8]. Figure 2 illustrates the doping profile in the 35 nm reference device and in each of the scaled devices. The simulated I_D-V_G characteristics of the reference device are in excellent agreement with measured data, as shown in Figure 3. The increased doping concentrations in the channels of the scaled devices are evident in Figure 2, and provide the required short channel control in the 25 nm or 18 nm devices.

For our statistical study we have simulated samples of 200 n-type MOSFETs with L_G of 35, 25, and 18 nm, using an integrated device simulation methodology [9]. The subthreshold current variation increases dramatically with the decrease in L_G. Figure 5 shows the increase in standard deviation of the V_T as L_G decreases. Figure 8 shows the percentage deviation of I_D in the subthreshold regime, and at saturation, as a function of L_G. The variations are larger in the subthreshold regime at the gate voltage V_G=50 mV. It is clear that intrinsic parameter fluctuations increase as conventional MOSFETs approach their scaling limit. Since the current distributions are far from normal in subthreshold, we present the 3rd and 4th moments of the current distributions in the saturation and subthreshold regions in Figures 9 and 10. There is a significant skew and change of peak shape away from the normal distribution for the subthreshold current shown in Figure 7. In general the distribution of the I_{on} and the logarithmic distribution of the I_{off} closely follow a normal distribution.

In summary, we have shown that intrinsic parameter fluctuations induced by discrete random doping in the channel region increase significantly at the scaling limits of MOSFETs, when real devices corresponding to the next three technology nodes are examined.

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A full journal publication of this work will be published in the Journal of Computational Electronics.

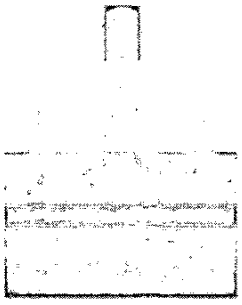

Fig.1 2-D Channel profile of In dopants in the simulated 35nm device.

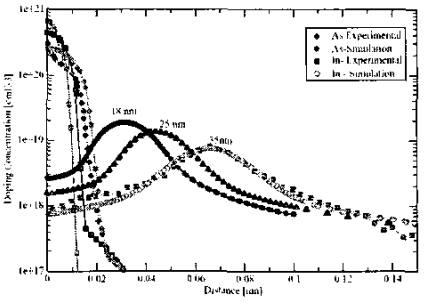

Fig.2 1-D Channel doping profiles of calibrated 35, 25 and 18nm scaled devices.

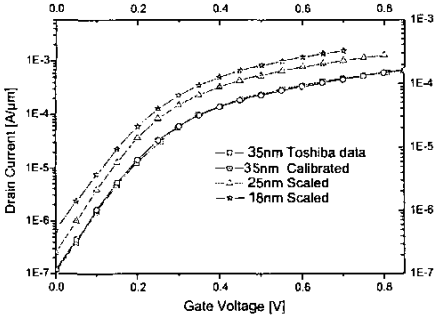

Fig. 3 I_D-V_G of 35nm 25, 18nm scaled devices at high V_D

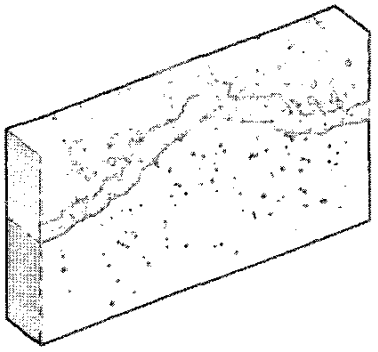

Fig. 4 3D-Potential distribution in a 35nm 'atomistic' device

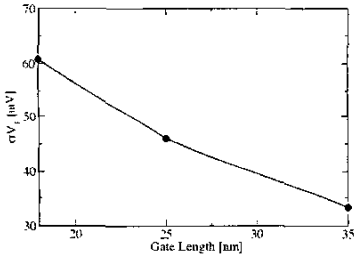

Fig. 5 V_T variation as a function of scaled device gate length.

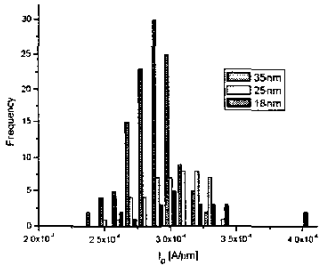

Fig. 6 I_D distribution of calibrated and scaled atomistic devices @V_G=850mV

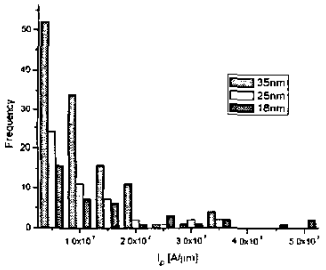

Fig. 7 I_D distribution of calibrated and scaled atomistic devices @V_G =50mV

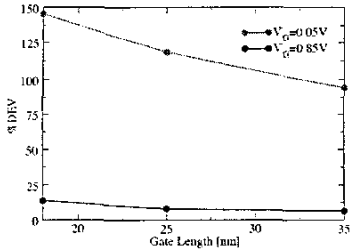

Fig. 8 Percentage deviation of I_D of the subthreshold and saturation regions @ V_G= 50 and V_G =850 mV respectively.

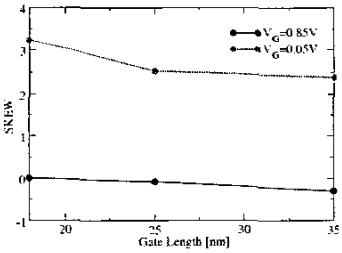

Fig. 9 Skew of I_D distribution of the subthreshold and saturation regions at the V_G = 50 and V_G =850 mV respectively.

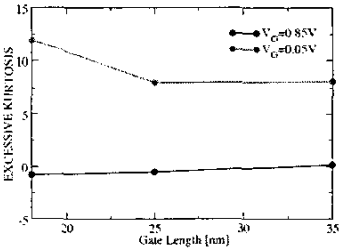

Fig.10 Kurtosis of I_D distribution of the subthreshold and saturation regions at the V_G = 50 and V_G =850 mV respectively.

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